

Design of Log Domain Low Pass Filters Using Quasi Floating Gate MOSFET

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Abstract—This paper presents the design of low voltage analog filters and highlights its comparison with FGMOS and QFGMOS. Though BJTs offer higher transconductance and high frequency response but do not favor device down scaling and high integration. Therefore CMOS version of log-domain filters is desired. In this paper we have discussed the sub-threshold behavior of MOSFET where it functions as translinear device and exhibits non-linear characteristics with low currents, hence useful for low power and low frequency applications. Comparison of first order log domain low pass filter with different topologies (Conventional MOSFET, FGMOS and QFGMOS) is also presented. The log-in and log-out circuits are used along with integrators to implement first order low pass filters. The proposed first order log domain low pass filter with inverting and non-inverting integrator exhibits bandwidth of 137.084 MHz and 631 MHz respectively with the supply voltage of 1V and capacitor chosen is of 2.0 pF and first order FGMOS and QFGMOS based log domain low pass filter with inverting integrator has bandwidth of 137.084 kHz and 179.236 MHz respectively. The performance of these circuits has been verified through PSpice simulations using level 3 parameters in 0.13 μm technology with supply voltage of 1V.

Keywords— Log domain low pass filters; sub-threshold; integrator; trans-linear.

I. INTRODUCTION

The process of filtering is usually performed by linear time invariant systems with a linear relationship between input and output signals. There is no restriction on the internal variables of the system which implies that the internal variables may be related in any manner and need not to have linear relations only. Therefore, the filtering process can be done by nonlinear functions among the internal variables of the filtering system. The internal variables may be chosen to be logarithmically and exponentially related so that the overall operation becomes linear. Thus, a filter based on nonlinear internal processing of signals involving logarithmic and exponential functions is referred to as log-domain filter. This technique employs the naturally occurring exponential relationship between the collector current and base emitter voltage of bipolar junction transistor (BJT) or MOSFETs operating in weak inversion region. Though BJTs offer higher transconductance and high frequency response but are not much subjected to down scaling, therefore, MOS versions of log-domain filters is necessary for integration. All BJT log-domain filters can be implemented in CMOS by replacing BJTs with MOSFETs biased in sub-threshold region. The sub-threshold MOSFET acts as translinear element exhibiting non-linear characteristics with low currents, hence useful for low power and low frequency applications.

Therefore, log-domain filtering is considered as a method of designing analog continuous-time filters with a linear transfer function between input and output terminal variables where as the signals at all nodes inside the circuit are assumed non-linear. That is, log domain filters are internally nonlinear and externally linear filters [1]. The concept of log domain filtering was first introduced by Adam's [2] in the 1970's but it require nearly ten years in establishing the fundamental

principles of log domain circuit design. It was only recently that the idea was expanded by Frey into a general filter design approach [3]. In log domain filtering technique, transistors need not be linearised as compression is followed by expansion. The additional advantage of Log Domain filter is their greater bandwidth which is due to low intermediate nodes. Log domain filters have input and output as current signals, which classify them as current-mode circuits. In this paper we have implemented log domain first order low pass filter with different topologies i.e. Conventional MOSFET, FGMOS, QFGMOS. The log-in and log-out circuits are used along with integrators (inverting and non-inverting) to implement first order low pass filters. And comparison between these topologies is also presented.

II. PRINCIPLE OF LOG DOMAIN FILTERS

The principle of operation of log domain circuits is based on instantaneous companding where the signals in current form with large dynamic range are compressed logarithmically during transformation into voltages and later expanded exponentially when converted back into current form. Therefore, log domain technique is very well suited to the implementation of continuous-time analog signal processing circuits that have to operate at very low supply voltages. The schematic of the log domain filter is shown in Fig.1 which comprises of three non-linear building blocks namely the compressor, the logarithmic filter and the expander.

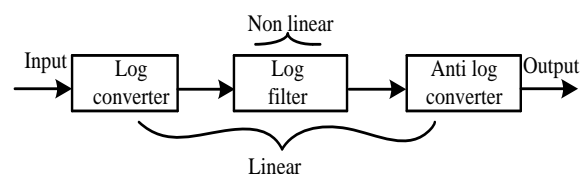


Fig. 1 Basic log domain filter.

III. LOG DOMAIN BUILDING BLOCKS

The basic building blocks of any log domain circuit are compressor and expander circuits which are also called Log-in and Log-out circuits respectively as shown in Fig. 2 (a & b) [4].

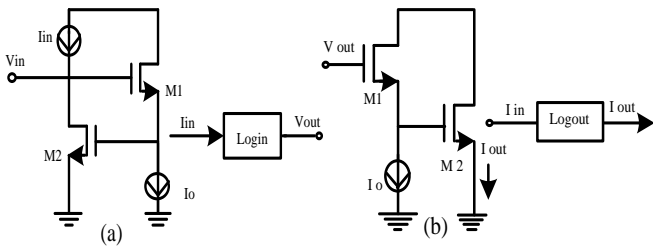


Fig. 2 (a) Log-in circuit (b) Log-out circuit.

Current mode log domain filters can be designed using voltage mode techniques if the compressed log domain voltages are chosen as the signal variables of the filter. In the log-in circuit, the input current signal is compressed through log mapping and is transformed into voltage. In order to obtain linear response, an exponential output circuit is required that is log-out circuit. With this circuit, the compressed voltage is expanded and transformed back to current form. Therefore, many voltage mode circuits can be transformed into current mode log domain versions through the above transformation circuits. The overall relationship between the input and output variables remains the linear as required for filter applications.

IV. FORMS OF LOG DOMAIN INTEGRATOR

Log domain integrators form the basis of log domain filtering technique. There are two types of log domain integrators namely inverting integrator and non inverting integrator [4] shown in Fig.3 (a) and (b) respectively. Here bias current provides tunability for log domain filters.

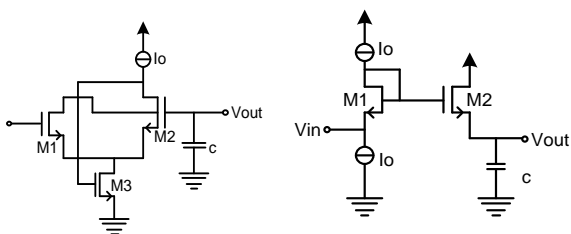


Fig. 3 (a) Inverting integrator (b) Non inverting integrator.

V. FIRST ORDER LOG DOMAIN FILTER WITH NON-INVERTING INTEGRATOR

A first order low pass filter including log-in and log-out circuits with non inverting integrator is shown in Fig. 3 [4]. The log-in and log-out circuits are used to make circuit linear with respect to both current input and output variables. The log-in circuit is interfaced at the input of the filter to perform current to voltage conversion and compression while log-out circuit is interfaced at the output of the filter to perform a voltage to current expansion. The first order log domain low pass filter with non inverting integrator has been simulated

for level 7 PSpice parameters for 0.13 μm technology with supply voltage 1V and I_{in} is 10 μA . The magnitude response of first order log domain low pass filter is shown in Fig. 4. The simulation results shows that pass band gain is 0 dB and -3 dB cut-off frequency is 631 MHz.

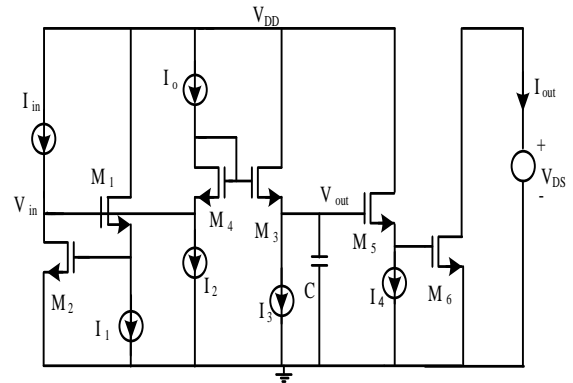


Fig. 3. First order log domain low pass filter.

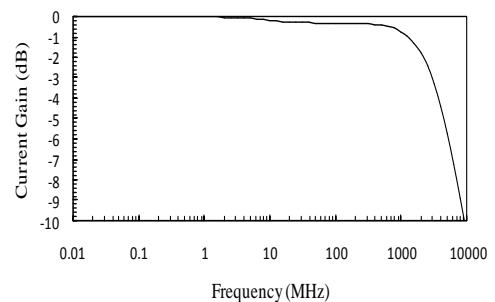


Fig. 4. Magnitude response of first order log domain low pass filter.

VI. FIRST ORDER LOG DOMAIN FILTER WITH INVERTING INTEGRATOR

In order to lose bandwidth and get better frequency response in stop band we replace non inverting integrator with inverting integrator. A first order low pass filter including log-in and log-out circuits with inverting integrator is shown in Fig. 5. Non inverting based first order log domain filter shown in Fig.3 has larger bandwidth than filter with inverting integrator [5].

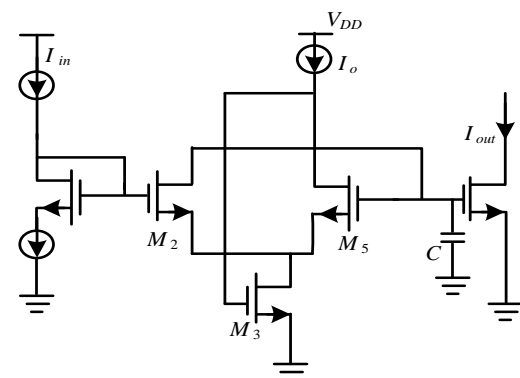


Fig. 5. First order log domain low pass filter with inverting integrator.

The first order log domain low pass filter with inverting integrator has been simulated for level 7 PSpice parameters for 0.13 μm technology with supply voltage 1V and I_{in} current is 10 μA . The magnitude response of first order log domain low pass filter is shown in Fig. 6. The simulation results shows that pass band gain is 0 dB and -3 dB cut-off frequency is 137.084MHz.

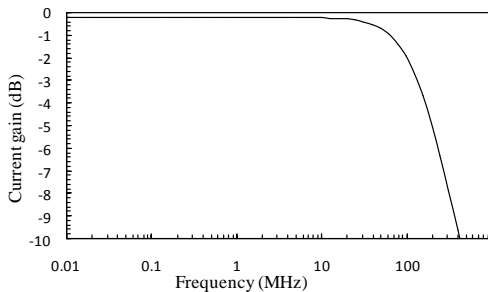


Fig. 6. Magnitude response of first order log domain low pass filter.

VII. FIRST ORDER FGMOS BASED LOG DOMAIN FILTER WITH INVERTING INTEGRATOR

A first order FGMOS based low pass filter including log-in and log-out circuits with inverting integrator is shown in Fig. 7. FGMOS based log domain low pass filter with inverting integrator offers even less bandwidth than conventional MOSFETs to provide better frequency response in stop band.

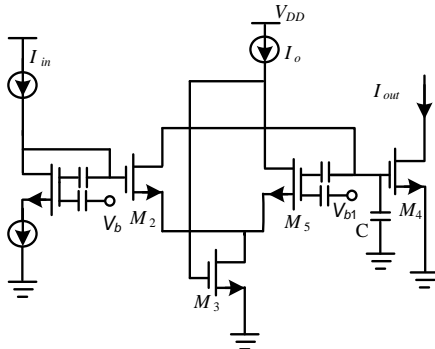


Fig. 7. First order FGMOS based log domain low pass filter.

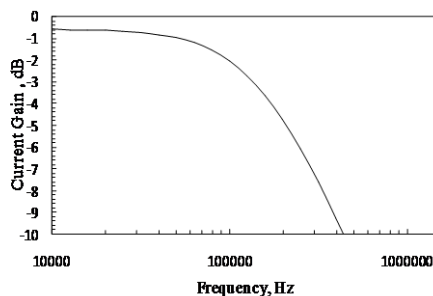


Fig. 8. Magnitude response of FGMOS based first order log domain low pass filter.

The first order FGMOS based log domain low pass filter with inverting integrator has been simulated for level 7 PSpice

parameters for 0.13 μm technology with supply voltage 1V and I_{in} current is 10 μA . The magnitude response of first order log domain low pass filter is shown in Fig. 8. The simulation results shows that pass band gain is 0 dB and -3 dB cut-off frequency is 137.084 kHz.

VIII. FIRST ORDER QFGMOS BASED LOG DOMAIN FILTER WITH INVERTING INTEGRATOR

A first order QFGMOS based low pass filter including log-in and log-out circuits with inverting integrator is shown in Fig. 9. QFGMOS offers better performance than FGMOS in terms of frequency response and needs less chip area. QFGMOS offers high bandwidth and low power dissipation and yields high value of resistance as compared to its FGMOS counterpart.

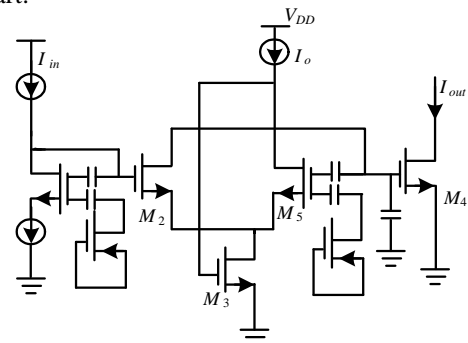


Fig. 9. First order QFGMOS based log domain low pass filter.

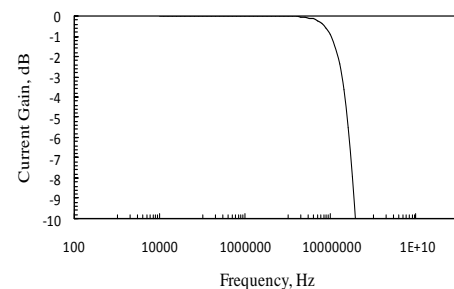


Fig. 10. Magnitude response of first order QFGMOS based log domain low pass filter.

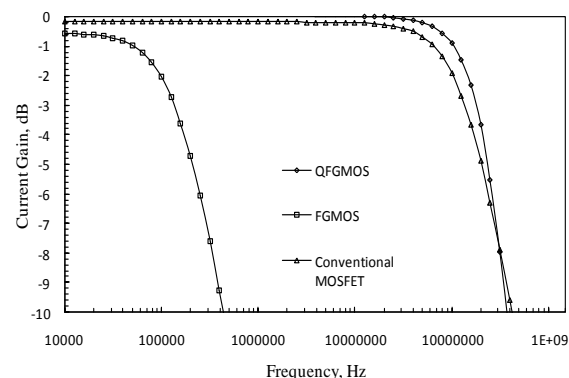


Fig. 11. Frequency response of different topologies of first order log domain low pass filters.

The first order QFGMOS based log domain low pass filter with inverting integrator has been simulated for level 7 PSpice

parameters for 0.13 μm technology with supply voltage 1V and I_{in} current is 10 μA . The magnitude response of first order QFGMOS based log domain low pass filter is shown in Fig. 10. The simulation results shows that pass band gain is 0 dB and -3 dB cut-off frequency is 179.236MHz.

The comparative frequency response different topologies of log domain low pass filters is shown in Fig. 11. The effect of different topologies on filter performance is shown in Table I.

Table I. Effect of different topologies on filter performance.

Topology	I_{in}	I_{out}	f_{-3dB}
Conventional MOSFET (non inverting)	10 μA	9.91 μA	631MHz
Conventional MOSFET (inverting)	10 μA	9.78 μA	137.084MHz
FGMOS	10 μA	9.35 μA	137.084kHz
QFGMOS	10 μA	10 μA	179.236MHz

IX. CONCLUSION

In this paper, we have presented different topologies of log-domain low pass filter. Inverting and non inverting integrator are used along with log-in and log-out circuits to

realize a first order filter. Non inverting integrator offers greater bandwidth, so in order to improve frequency response in stop band we use inverting integrator. Further first order log domain low pass filter can also be simulated with FGMOS and QFGMOS. Comparison of different topologies of log-domain low pass filter has also been presented. These circuits utilize grounded capacitors which are desired for integration point of view since they occupy less chip area. The behavior of filter circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 μm CMOS technology with a supply voltage of 1 V.

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