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Fabrication and Characterization of Ge Based Nano MOS Capacitor

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***Abstract*—**In the beginning of 21st century, many new electronic materials have been explored and incorporated into silicon CMOS transistors for enhancing their device performance and energy-efficiency. Beside silicon, germanium is another interesting candidate for nanoscale CMOS technology as it offers the mobility for electrons and holes exactly two and four times relative to Silicon. However, many issues still need to be addressed before Ge can be implemented in high-performance field-effect-transistor (FET) devices. One of the key issues is to provide a high-quality interfacial layer. In this paper various methods for Ge surface passivation (e.g. surface oxidation and nitridation), various high-*k* dielectrics materials, and deposition methods have been examined to attain proper interfacial properties. Further, fabrication and characterization of MOSCAP structures such as Al/HfO_2/Ge has been presented. The deposition of HfO_2 on Ge substrate has been studied using atomic layer deposition (ALD) Different characterization techniques have been used to analyze these gate stack structures for the calculation of equivalent oxide thickness (EOT), dielectric constant (k), effective oxide charges/fixed oxide charges (Q_{eff}) and interface trap density (D_{it}). Ge MOS capacitors were successfully fabricated by depositing thin film of hafnia by ALD methods. The leakage current density, C–V hysteresis, charge trapping and interface state density can be significantly reduced by the surface nitridation of the Ge and also inhibits the formation of interfacial layer

***Keywords*—**MOS capacitor; Surface passivation; Dielectric constant; EOT.

I. INTRODUCTION

Today, the modern human society is becoming comfortable for high technology electronic products such as personal computer, mobile phones, video game machines, digital cameras, and human-like robots etc. by making use of ultra large scale integration (ULSI) technology. The silicon metal oxide semiconductor field effect transistor (MOSFET) has been the most essential building block of current ULSI integrated circuits (ICs) since its invention in the 1960s. The performance of silicon ULSI depends on the capability of the MOSFET, especially the processing speed and electrical power dissipation which are hanged on its geometrical size. The semiconductor industry has been loyally following Moore's law to regularly improve the performance and intricacies of ICs [1]. However, as silicon begins to reach its fundamental limits, even greater barriers need to be overcome where the use of more novel materials and device structures may be needed to continue CMOS scaling. Possessing extraordinary qualities such as low leakage current, low interface state density and good thermal stability, silicon (Si) has been used in MOS technology for many decades [2]. As per Moore's law, achieving high device density and faster switching speed will cause transistor gate length to shrink and reach around 7-5 nm by year 2020-2022. This results in dwindling of gate length and gate oxide thickness to 1 nm and ultimate oxide scaling down to EOT (Equivalent oxide thickness) of approximately 0.5 nm is required [3].

Recently, many new electronic materials have been explored and incorporated into silicon CMOS transistors. As this trend continues, it is expected that most of the non silicon materials will substitute silicon as the ultimate transistor channel material [4]. To review the physical limits, microelectronics revolution has followed the non-silicon technology due to the possession of their excellent carrier transport properties, including carbon-based semiconductors such as carbon nanotubes [5], [6], graphene [7], [8], germanium (Ge) [9], [10] and III-V compound semiconductors [11], [12]. High mobility channel materials such as Ge and III-V compounds offer a potential solution to meet the power and performance specifications of future CMOS nodes. Beside silicon, germanium is an interesting candidate for nanoscale CMOS technology as it offers the mobility for electrons and holes exactly two and four times relative to Silicon. Reported room temperature hole mobility in a 7.5 nm thick Ge quantum well has exceeded 2500 cm^2/V-sec [13]. High performance, n and p-channel Ge MOSFETs has been reported [14-19]. These alternate channel materials can enhance channel mobility beyond the physical limits of Si based MOS devices [20].

During the past years, many approaches have been examined to passivate the Ge surface. Surface nitridation of Ge was an early attempt, since GeO*x* was usually considered as a poor and unstable oxide. Epitaxial Si passivation of Ge surfaces has been well established and high performances were demonstrated for p-MOSFET devices. S passivation was effective for III–V compound semiconductors and was also investigated for Ge. Recently, GeO_2 interfacial layer (IL) exhibit promising properties as well. We will review those passivation methods and summarize the results from the existing literature. Many high-k oxides have been comprehensively studied as a possible replacement for conventional SiO_2 such as Al_2O_3 [21-22], HfO_2 [23], TiO_2 [24], CeO_2 [25], $LaAlO_3$ [26], HfSiO [27], ZrO_2 [28]. The deposition of a high-*k* dielectric can be achieved by various methods, including physical vapor deposition (PVD), molecular beam deposition (MBD) [29], chemical vapor

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deposition (CVD), and atomic layer deposition (ALD) (thermal and plasma). Among these techniques, ALD received great interest due to its intrinsic self terminated growth nature. ALD is a cyclic deposition process that consists of sequential self-limited surface adsorption and reaction. It provides precise thickness control at the atomic level, which makes it the dominant deposition technique for high-*k* dielectrics in current MOS devices.

Among these high-k materials, HfO_2 has been identified as promising candidate to meet the scaling requirements because of its high dielectric constant (20-25), high band gap (5.8 eV), superior thermal stability with silicon, low density of interface states and good electrical reliability. In order to obtain good electrical properties, a thin EOT and a thermally stable oxide layer, the fabrication of high k/Ge gate stacks have been reported due to the higher mobility of Ge. It has been seen that the interface layer between high-k dielectric film and Ge is much thinner than that between Si and a high-k dielectric film.

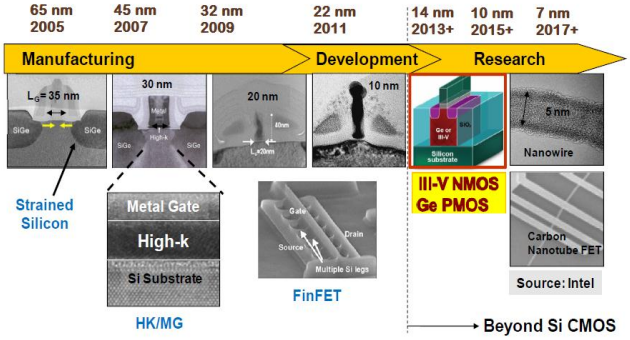

Fig. 1. TEM images of MOSFET scaling over the years with technological advances labeled (Source: Intel corp, USA).

The formation of GeO_2 on Ge was the biggest hindrance during the past few years for the fabrication of CMOS devices. There is also the problem of diffusion of Ge into HfO_2 which causes device instability, high interface state density D_{it} and mobility degradation. Thus, in order to suppress the intrinsic GeO behavior, the nitridation of GeO_2 (GeON) is required. In order to improve these parameters further, nitridation of GeO_2 i.e., GeON IL has been suggested for enhancing its electrical properties. In this work, high k HfO_2 films has been deposited on two different ILs (GeO_2 and GeON) for Ge gate stacks by ALD with thickness of 9.77 nm. The thickness of film was evaluated by Spectroscopic Ellipsometer (SE) and Filmetrics Reflectometer whereas the states of the elements and chemical compositions of the films were studied by X-ray Photoelectron Spectroscopy (XPS). High-frequency Capacitance-Voltage (C-V), Conductance-Voltage (G-V) and Current-Voltage (I-V) measurements were used to obtain the electrical properties of the Al/HfO_2/Ge MOS capacitor.

II. Experimental Details and Fabricated Structure

2" p-type Ge wafers having orientation <100> and 1-10 Ω-cm resistivity were used as substrates. Germanium dioxide (GeO_2) and germanium oxynitride (GeON) were used as surface passivation layers prior to the HfO_2 dielectric deposition. For surface nitridation, the initial oxide present on the Ge substrate was removed using a cyclic rinsing of acetone, IPA and de-ionized water followed by a rinse in 5:1 HF solution three times for 30 sec each and then blown dry in N_2 gas. ANNEALSYS AS-ONE 150 RTP system was used for oxidation and nitridation of these samples for 3 minutes at 400°C in O_2 and 600 °C in NH_3 ambient respectively. After the surface passivations, the Ge wafers were immediately transferred to a high vacuum ALD system (Nanotech Fiji 200) and deposition of HfO_2 was performed at 200°C using alternating surface-saturating reactions of $HfCl_4$ and H_2O precursors. Each precursor was pulsed for 2 second and N_2 purging was done for 30 seconds after H_2O and 60 seconds for $HfCl_4$ pulse.

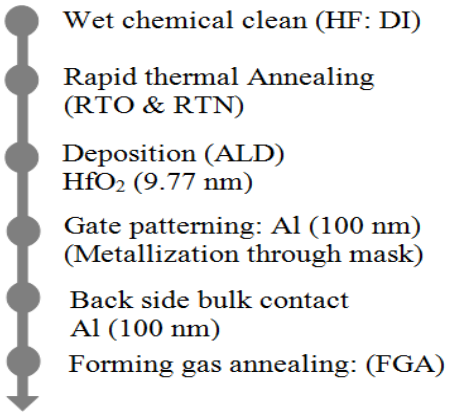

Fig. 2. Fabrication process flow for Al/HfO_2/ILs/Ge p-MOS capacitor.

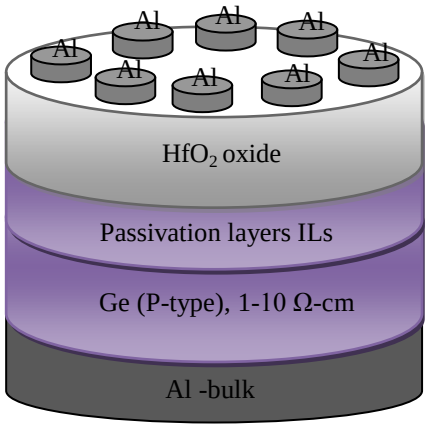

Fig. 3. Schematic of Al/$Hf0_2$/ILs/Ge p-MOS capacitor.

The thickness of HfO_2 was found to be about 9.77 nm as measured by an ellipsometer (SE 800) and filmetrics reflectometer. After that, a 1000 Å thick layer of aluminum (Al) was deposited using thermal evaporator-Al system through a shadow mask to pattern the capacitor electrode on the top hafnia layer to fabricate MOS capacitor structure for electrical properties measurements. Before the back contact formation, the buffered hydrofluoric acid (BHF) followed by three times rinsed in de-ionized water was used to remove the

Rakesh Prasher and Rakesh Vaid , "Fabrication and characterization of Ge based nano MOS capacitor", *Journal of Scientific and Technical Advancements*, Volume 1, Issue 3, pp. 203-207, 2015.

native oxides. By thermally evaporating Al metal, an ohmic contact was formed on the backside of Ge substrate to form MOS capacitor. Finally, forming gas anneal (FGA) at 420 °C for 20 minutes using 96% N_2 and 4% H_2 ambient was performed with the fabricated Al/HfO_2/ILs/Ge MOSCAP structure. X-Ray photoelectron spectroscopy (XPS) was used to analyze the states of the elements and chemical compositions. C-V, G-V and I-V measurements of fabricated MOS structures were performed to extract various electrical parameters using electrical characterization tool (VEGA). The complete process flow of Al/HfO_2/ILs/Ge p-MOS capacitor fabrication is illustrated in fig. 2 and schematic of the Al/HfO_2/ILs/Ge p-MOS capacitor is shown in fig. 3.

III. Results And Discussion

In this paper, the effect of interfacial layers between HfO_2 and Ge on the physical as well as electrical characteristics of Al/HfO_2/ILs/Ge p-MOS capacitor has been discussed. We used oxidation for 3 minutes at 400°C in O_2 ambient and nitridation for 3 minutes at 600 °C in NH_3 ambient for surface passivation. Further the effect of forming gas annealing has also been discussed.

Thickness of HfO_2 Layer

The thickness of the HfO_2 film was found to be 9.77 nm measured using variable angle spectroscopic ellipsometry and also by the filmetrics Reflectometer for the confirmation of the exact value. The thickness was calculated by taking the mean of all the values from both the methods. The refractive index for the deposited films was found to be in the range 2.12 - 2.42. The equivalent oxide thickness (EOT) with GeON as IL has been found to be 3.23 nm while with GeO_2 as IL, the value of EOT found was 3.67 nm. These EOT values were determined using physical thickness of HfO_2 layer and dielectric constant calculated from the capacitance voltage (CV) measurements.

X - Ray Spectroscopy

In fig. 5, the sample presents two Ge3d peaks at 28eV and 31eV and Ge3d XPS spectrum obtained from GeO_2 grown at 400°C displays the presence of bonded oxygen in the state (sub-peak with 3.2 eV shift in binding energy from Ge3d peak) which confirmed the growth of GeO_2 as the initial dielectric. The shifting of sub-peak towards the lower binding energy shows the presence of nitrogen atoms due to the nitridation of GeO_2 and changes in its chemical state converting it into GeON. Fig. 5 shows the XPS depth profile of 9.77 nm thick HfO_2 diectric material on Ge substrate. In Fig 4 (d), when sample was scanned from the top, it displays two peaks at 16 eV and 17.7 eV which correspond to Hf4f peaks. On increasing the sputter depth, Ge3d region shows the presence of Ge-O, GeO_2 and GeON peaks from the Ge substrate and confirmed the existence of Oxygen and Nitrogen atoms in the HfO_2/Ge interlayer. O1s peak was detected at 529.25 eV as shown in figure 5 (b) and two peaks of N1s at 396.25 eV and 399.5 eV were also detected as shown in figure 5 (c) from the sample of HfO_2/GeON/Ge stack. These peaks suggest the formation of germinate of hafnium ($HfGeO_2$/HfGeON).

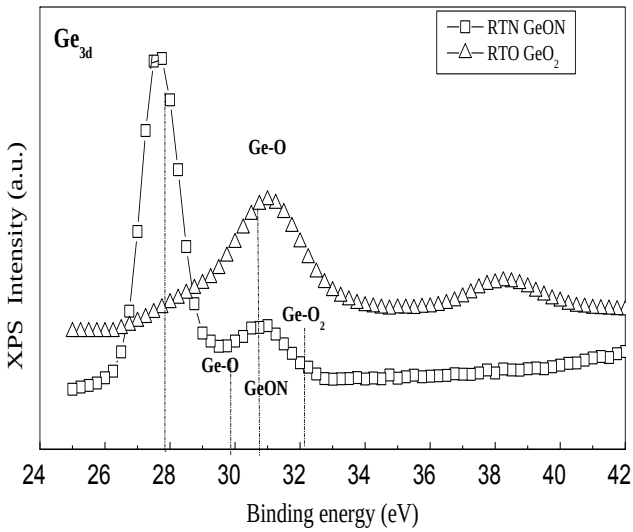

Fig. 4. XPS spectra of Ge3d for GeO_2 and GeON.

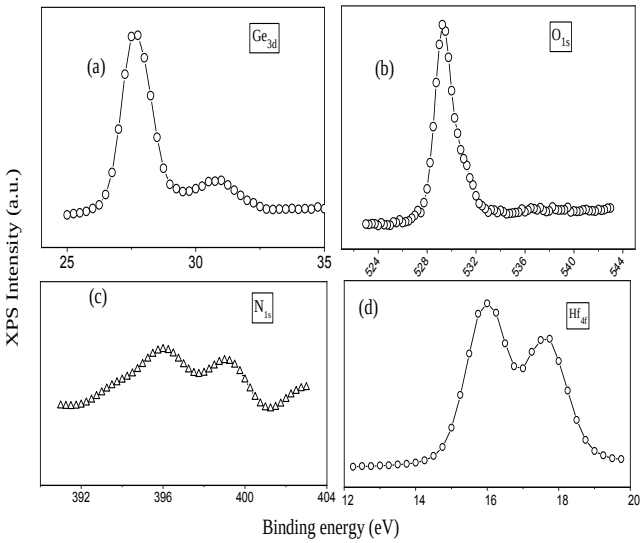

Fig. 5. (a) Ge3d (b) O1s (c) N1s and Hf4f XPS depth profile of 9.77 nm HfO_2 dielectric on Ge substrate.

Effect of Interfacial Layers (ILs) on Electrical Characteristics

The normalized capacitance–voltage (C-V) curves for Al/HfO_2/Ge p-MOS MOS capacitors for different interfacial layers at a frequency of 100 KHz were measured to verify the dielectric behavior of HfO_2 films. C-V characteristics of the devices with as ALD-deposited 9.77 nm HfO_2 film and GeO_2/GeON ILs between HfO_2 and Ge substrate demonstrate typical MOS capacitor behavior. Comparison of C–V characteristics of MOSCAPs with Al/HfO_2/Ge stack for two interfacial layers (ILs) with controlled sample is shown in fig. 6. As shown in this figure, the dc gate bias voltage was swept from a negative voltage to a positive voltage and then returned to the initial value (-3V to 1V). There occurs a positive shift for the flat band voltage with the increase in the annealing

Rakesh Prasher and Rakesh Vaid , "Fabrication and characterization of Ge based nano MOS capacitor", *Journal of Scientific and Technical Advancements*, Volume 1, Issue 3, pp. 203-207, 2015.

temperature. Both interfacial layered HfO_2/Ge stack shows better curves than controlled sample because of the improvement of interfacial trap density by the interfacial layer. For HfO_2/GeON IL/Ge stack, a reduction in hysteresis window is seen as the traps have experienced an effective suppression. In accumulation region of C-V curve, the accumulation capacitance is observed to be increased the HfO_2/RTN GeON IL/Ge stack because of the improvement of interfacial trap density (D_{it}) of the interfacial layer. Leakage is clearly visible in accumulation region in case of controlled sample which means as deposited HfO_2 layer is due to trap charges. The value of dielectric constant (k) of the HfO_2 was extracted from the accumulation region of C–V curve in fig. 5. The calculated value of dielectric constant for HfO_2/RTN GeON IL sample is fund to be 13. The lower dielectric constant may be due to presence of trap charges in the film that decides the quality of the film. In this Figure, flat band voltage V_{fb} shifted toward the negative voltage has been observed for interfacial layers stack and was due to the existence of the positive effective oxide charge (Q_{eff}) in the GeO_2/GeON ILs and HfO_2. Calculated value of Q_{eff} in our work for three different samples of RTN GeON, RTO GeO_2 ILs and controlled sample are 16.92×10^{12} cm^{-2}, 17.55×10^{12} cm^{-2}, 11.5×10^{11} cm^{-2}.

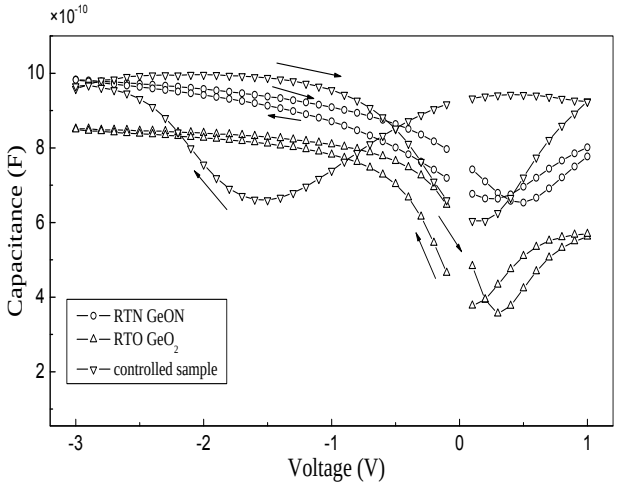

Fig. 6. Caparison of C-V characterstics for RTN GeON and RTO GeO_2 ILs with controlled sample measured on Al/HfO_2/Ge p-MOS capacitor at 100 KHz frequency.

The effect of interfacial layers on interface trap density (D_{it}) & effective oxide charges (Q_{eff}) has been listed in table 1. The value of D_{it} of the HfO_2 was extracted from the accumulation region of C-V curve in fig. 6 and inversion region of G-V curve. The calculated values are 19.282×10^{13}, 2.53×10^{13} and 0.63×10^{12} eV^{-1} cm^{-2} for controlled (HfO_2/Ge), HfO_2/GeO_2/Ge & HfO_2/GeON/Ge samples respectively. It has been observed that a lower D_{it} and less EOT were achieved for HfO_2/GeON/Ge sample, which helps in the improvement of leakage current of the device. It clearly shows that HfO_2/GeON/Ge sample leads to significant reduction in the D_{it} at the expense of a slight increase in Q_{eff}. The computed values of hysteresis from capacitance–voltage characteristics for each sample are given in table 1. This significant shift in C–V hysteresis for GeON and GeO_2 ILs samples as compared to controlled sample indicates the improvement in dielectric layer, reduction in equivalent oxide thickness (EOT), reduction in interface trap density (D_{it}), reduction in fixed oxide charges or effective oxide charges (Q_{eff}). These properties decide the quality of the MOS capacitor. From this table it is concluded that the Al/HfO_2/Ge p-MOS capacitor with very small C–V hysteresis and low gate leakage has been achieved with GeON interfacial layer.

Table 1. Key properties of different gate stack for Al/HfO_2/Ge p-MOS Capacitor.

Dielectric properties	**Controlled sample**	**RTO GeO_2/HfO_2**	**RTN GeON/HfO_2**
D_{it} (eV^{-1} cm^{-2})	1.928×10^{14}	2.53×10^{13}	6.3×10^{11}
Thermal stability	Stable	Unstable	Stable
Dielectric constant	11.6	11.4	13
Q_{eff} (cm^{-2})	1.15×10^{12}	1.75×10^{13}	1.69×10^{13}
EOT (nm)	3.27	3.67	3.23

IV. Conclusion

Thin film of hafnia with thickness of 9.77 nm was successfully deposited on n-type Ge substrate by ALD method. Physical and electrical characterization of the HfO_2 thin film MOS capacitor with FGA at 420 °C temperature has been studied. Thickness of hafnia is determined by ellipsometer and profilometer. This study suggested that before deposition of HfO_2 on Ge, surface must be mandatory which help us in improvement of overall nano device performance.

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