International Journal of Scientific and Technical Advancements
IJSTA
ISSN: 2454-1532

Simulation Study of Coaxially Gated Ballistic CNTFET

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***Abstract*—**Low power consumption and high performance of electronic devices are highly demanded in a recent days therefore the semiconductor industry and academia have to push the downscaling of MOSFET to achieve these requirements. To extend Moore's Law further into the next decade, it is absolutely necessary that Silicon advantages may be combined with the other novel nanotechnologies onto the same Silicon platform. It is therefore important to search for alternative of Si-MOSFET devices. Because of the capability of ballistic transport, CNTFET have been studied as a potential alternative to CMOS devices in future. In this paper we have studied the performance of a ballistic carbon nanotube field effect transistor and the results have been compared with the 15nm n-MOSFET and 60nm Tri gate n-MOSFET. It has been concluded that the ballistic CNTFET has high drive current (I_{on}), low leakage current (I_{off}), high transconductance, high I_{on}/I_{off} ratio (fast switching speed), improved short-channel effects such as Subthreshold Slope (SS) and Drain Induced Barrier Lowering (DIBL).

***Keywords*—** Carbon nanotube; CNTFET; insulator thickness; dielectric constant; threshold voltage.

I. INTRODUCTION

Moore's Law states that the number of transistors per integrated circuit doubles every 24 months, and it has been the guiding principle for the semiconductor industry for more than 40 years. The sustaining of Moore's Law, however, requires continual transistor miniaturization and performance improvement. Fig. 1 shows the logic technology node and the corresponding transistor physical gate length (L_G) versus year of introduction. It can be seen that the physical L_G has been scaled by more than 30% every 2 years. The physical gate length of the Si transistors used in the 90nm logic generation node is about 50nm, physical gate length of the Si transistors used in the 2009 nm logic generation node is about 15 nm and it is projected that the size of the transistors will reach about 10nm in the current technology node.

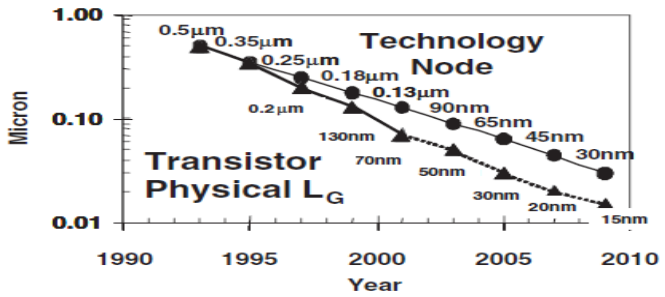

Fig. 1. Technology node and transistor physical L_G versus year.

Through silicon innovations such as strained-Si channels, high-K/metal-gate stacks, and the non-planar "Tri-gate" CMOS transistor architecture, CMOS transistor scaling and Moore's Law will continue at least through the middle of the next decade. By combining silicon innovations with other non-Si nanotechnologies on the same silicon platform, it is expected that Moore's Law will extend well into the next decade. Recently much progress has been made in the research of non-Si nanotechnology for future nanoelectronics applications. In particular, several emerging nanoelectronic devices such as carbon-nanotube field effect transistor (FET), semiconductor-nanowire FET, and planar III-V compound semiconductor FET, all hold promise as device candidates to be integrated onto the silicon platform for enhancing circuit functionality and for further extending Moore's Law. Semiconducting carbon nanotubes are an attractive and viable option for channel structures which show promise due to their superior electrical characteristics over silicon based MOSFETs. Since the electron mean free path in SWCNTs can exceed 1 micrometer, long channel CNTFETs exhibit near-ballistic transport characteristics, resulting in high-speed devices [1-5].

In this paper we have studied the performance of a ballistic carbon nanotube field effect transistor using a two-dimensional (2-D) simulation and the results have been compared with the 15nm N-MOSFET and 60nm Tri gate N-MOSFET in terms of On current (I_{on}), Off current (I_{off}), I_{on} / I_{off} ratio, transconductance (g_m), Subthreshold Slope (SS) and Drain Induced Barrier Lowering (DIBL).

II. TWO DIMENSIONAL MODEL

At low gate voltages, the energy barrier between the source and drain is high, and the device is off. A high drain bias lowers the energy in the drain, and when a high gate voltage lowers the potential energy barrier, electrons flow from source to drain. With respect to that the top of the energy barrier between the source and drain has special significance in operation of FETs. Therefore, it can be the good starting point for a model. Our key task in developing model will be to devise a simple approach to determine the self-consistent potential at the top of the barrier. The operation of MOSFETs in the ballistic regime has recently been explored by simple, analytical models as well as by detailed numerical simulations. The top of the energy barrier between the source and drain has

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ISSN: 2454-1532

special significance in operation of MOSFETs. Fig. 2 shows a typical band profile of MOSFET-like transistors. Carriers with energies above the top of the barrier are transmitted, and produce the source-drain current. Those with energies below the top of the barrier are reflected back into the source (drain) by the channel barrier. The +*k* states at the top of the barrier, therefore, are filled by the source Fermi level, and the -*k* states are filled by the drain Fermi level. To treat transistor electrostatics analytically, we adopt a capacitance model as shown in fig. 3. It consists of three capacitors, which represent the effect of the three terminals on the potential at the top of the barrier. The mobile charge is determined by the local density of states at the top of the barrier, the location of the source and drain Fermi levels μ_S or E_{F1} and μ_D or E_{F2}, and by the self-consistent potential at the top of the barrier U_{scf} [6-9].

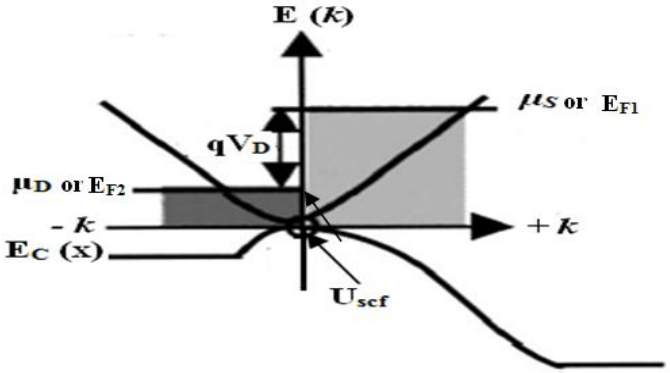

Fig. 2. Typical band profile of MOSFET-like transistors. At the ballistic limit, the + *k* states at the top of the barrier are filled by the source Fermi level and the – *k* states by the drain Fermi level.

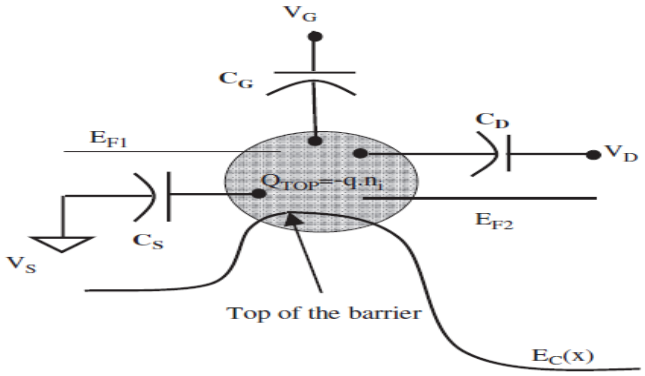

Fig. 3. Two-dimensional circuit model for a ballistic CNTFET. The potential at the top of the barrier, U_{scf}, is controlled by the gate, drain and source potentials through the three capacitors shown. The mobile charge at the top of the barrier is determined by U_{scf} and by the location of the two Fermi levels. The nonlinear semiconductor (or quantum) capacitance is not shown explicitly but is implicit in the treatment of band filling.

When the terminal biases are zero, the equilibrium electron density at the top of the barrier for the ith conduction band is

$$(n_0)_i = \int_{-\infty}^{\infty} D_i(E) f(E - E_F) dE \quad (1)$$

where f (E - E_F) is the equilibrium Fermi function, and D_i (E), the local density of states at the top of the barrier.

When a bias is applied to the gate and drain terminals the self-consistent potential at the top of the barrier becomes Uscf, and the states at the top of the barrier are now populated by two different Fermi levels. The + *k* states are populated by injection from the source and the - *k* states by injection from the drain. Therefore, the electron density at the top of the barrier for the ith conduction band is

$$n_i = \frac{1}{2}\int_{-\infty}^{\infty} D_i(E - U_{scf})[f(E - E_{F1}) f(E - E_{F2})] dE \quad (2)$$

where $E_{F1} = E_F$ and $E_{F2} = E_{F1}$-qV_{DS}.

Given an arbitrary density of states D_i(E) and the location of the source and drain Fermi levels, we can evaluate the electron density at the top of the barrier, n_i, if the self-consistent potential is known. The potential at the top of the barrier, U_{scf}, can be written as summation of the following two terms:

(1) The homo generous solution U_H that ignoring the presence of the mobile charge in the channel, and calculating the Laplace potential at the top of the barrier due to terminal biases, which is

$$U_H = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) \quad (3)$$

In this equation, the three α's describe how the gate, drain and source control the Laplace solution and are given by

$$\alpha_G = \frac{C_G}{C_T} \; \alpha_D = \frac{C_D}{C_T} \; \alpha_S = \frac{C_S}{C_T} \quad (4)$$

where C_T is the parallel combination of the three capacitors C_G, C_D, C_S.

(2) The particular (in homogeneous) solution UP that consists of grounding the three terminals and computing the potential due to the mobile charge at the top of the barrier, $\Delta n = n_i - (n_0)_i$, from

$$U_P = \frac{q^2}{C_T} \Delta n \quad (5)$$

Therefore, U_{scf} is equal to

$$U_{scf} = U_H + U_P = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + \frac{q^2}{C_T} \Delta n \quad (6)$$

Eqs. (2) and (6) represent two, coupled non linear equations for the two unknowns n_i and U_{scf}. These equations can be solved iteratively to find the carrier density and self-consistent potential at the top of the barrier. Finally, the drain current is evaluated from

$$I_D = \frac{2q k_B T}{\pi \hbar} \int_{-\infty}^{\infty} [f(E - E_{F1} - U_{scf}) f(E - E_{F2} - U_{scf})] dE \quad (7)$$

where the factors of 2 account for valley degeneracy, and k_B and $\hbar$ are Boltzmann and Planck constant, respectively

III. Device Structure

The structure of a coaxially gated n-type CNTFET is shown in fig. 4. The coaxial gate geometry offers the best electrostatic gate control. The intrinsic nanotube channel is separated from the source/drain metal contact by the heavily n-doped nanotube source/drain extension to minimize the Miller capacitance between gate and source/drain electrode. The source/drain region could also be realized by using weakly coupled metal–nanotube contacts with an appropriate metal work function. We assume that the metal–nanotube contact resistance, R_C = 0, and carrier transport through nanotube is ballistic (no scattering). Calculations based on these assumptions should establish the upper limit of CNTFET performance. The coaxial gate is placed around the intrinsic

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part of the nanotube and separated by a gate oxide of SiO_2 with thickness of 1.5 nm and dielectric constant of 3.9. Also, we analyze the CNTFET structure at room temperature (T = 300K). In this model, we obtained gate control parameter α_G = 1and drain control parameter α_D = 0.

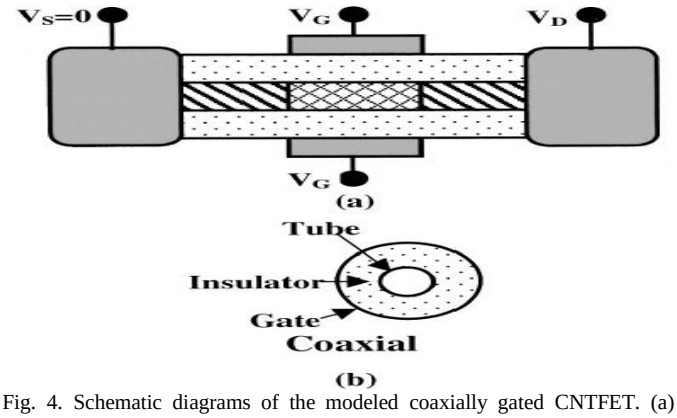

Fig. 4. Schematic diagrams of the modeled coaxially gated CNTFET. (a) Cross section along the nanotube channel direction. The hatched line regions are the heavily *N*-doped nanotube source and drain, and the thin crosshatched line region is the intrinsic nanotube channel. (b) Cross section perpendicular to the nanotube channel direction, which shows the gate configuration.

IV. Results And Discussion

In this paper, we have discussed the various simulation results of cylindrical shaped ballistic n–type CNTFET such as transfer characteristics, output characteristics, mobile charge, quantum capacitance/ insulator capacitance, average velocity, gm/Id ratio, drive current (I_{on}), I_{on} / I_{off} ratio, transconductance, output conductance, subthreshold slope (SS) and drain induced barrier lowering (DIBL) by choosing the parameters like CNT diameter d = 1 nm, threshold voltage V_{th} = 0.3 V, temperature T = 300 K, insulator thickness t_{ins} = 1.5 nm, gate insulator dielectric constant κ = 3.9 (SiO_2), gate control parameter α_G = 1, drain control parameter α_D = 0. All results are obtained using the nanohub simulator FETTOY [10].

A. Variation of Drain-Source Current (I_{DS}) with respect to Gate- Source Voltage (V_{GS})

The variation of drain-source current (I_{DS}) with respect to gate source voltage (V_{GS}) also called transfer characteristics of CNTFET as shown in fig. 5. It has been observed that the drain current of the CNTFET increases with the increase in drain-source voltage (V_{DS}). Also, it is evident from the figure that the transconductance of device improves with the increase in drain-source voltage (V_{DS}) due to more controllability of gate on the channel.

B. Variation of Drain-Source Current (I_{DS}) with respect to Drain-Source Voltage (V_{DS})

The variation of drain-source current (I_{DS}) with respect to drain-source voltage (V_{DS}) for various values of gate-source voltage (V_{GS}) is as shown in fig. 6. This is also called output characteristics. It has been observed that the saturation current increases with the gate-source voltage (V_{GS}) and degree of this positive effect increases as we go for higher gate-source voltage (V_{GS}). Also, it can be seen from the figure that the output conductance increases with the increase in gate-source voltage (V_{GS}).

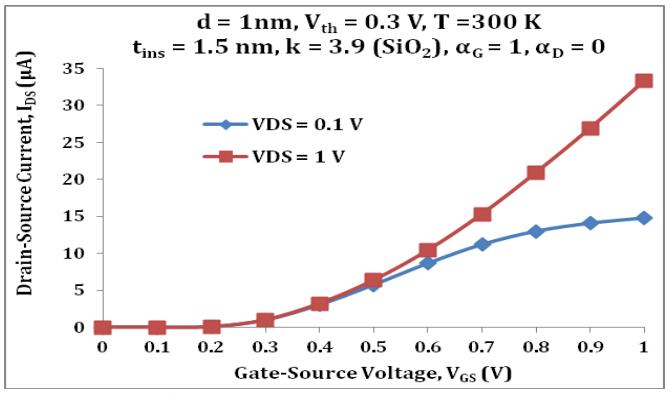

Fig. 5. Variation of drain-source current (I_{DS}) with respect to gate source voltage (V_{GS}) for various values of drain-source voltage (V_{DS}).

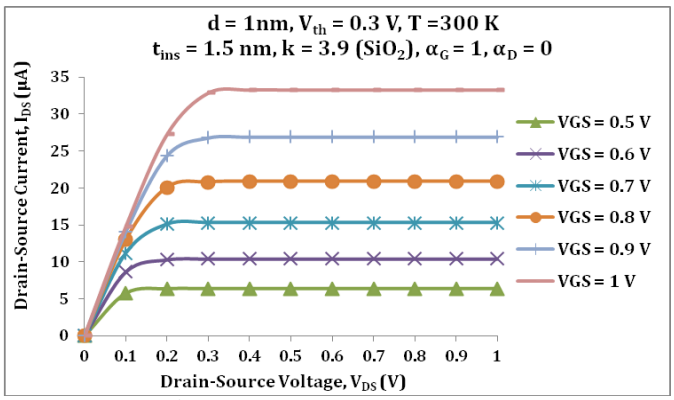

Fig. 6. Variation of drain-source current (I_{DS}) with respect to gate-source voltage (V_{GS}) for various for various values of gate-source voltage (V_{GS}).

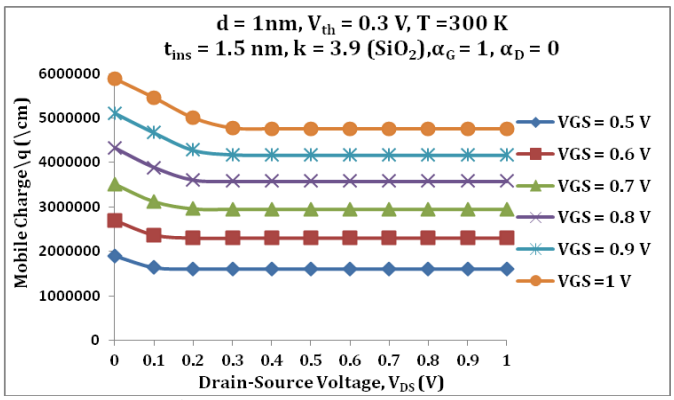

Fig. 7. Variation of mobile charge/*q* (/cm) with respect to drain- source voltage (V_{DS}) for various values of gate-source voltage (V_{GS}).

C. Variation of Mobile Charge/q with respect to Drain-Source Voltage (V_{DS})

The variation of mobile charge/q with respect to drain-source voltage (V_{DS}) for various values of gate-source voltages (V_{GS}) is as shown in fig. 7. It is noticed that increasing the drain voltage beyond a specific value has no longer an effect on the shape of the curves since the mobile charge remains constant. It is also observed that low drain voltage produces

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higher mobile charge and high drain voltage produces lower mobile charge. Also, it has been noticed that the mobile charge increases with the increase in reduction in gate-source voltage (V_{GS}).

D. Variation of Mobile Charge/q with respect to Gate-Source Voltage (V_{GS})

The variation of mobile charge/q w.r.t gate-source voltage (V_{GS}) for a drain- source voltage (V_{DS}) of 0.1V and 1 V is as shown in fig. 8. It has been observed that the mobile charge increases with the increase in gate source voltage beyond 0.2 V. Also, it is noted that with the increase of drain- source voltage the mobile charge increases.

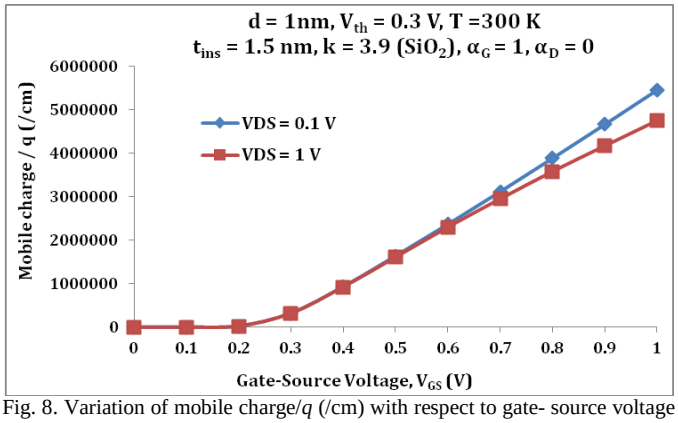

Fig. 8. Variation of mobile charge/*q* (/cm) with respect to gate- source voltage (V_{GS}) for a drain- source voltage (V_{DS}) of 0.1V and 1 V.

E. Variation of QC/Insulator Capacitance with respect to Gate Source Voltage (V_{GS})

The variation of QC/Insulator capacitance with respect to gate- source voltage (V_{GS}) for a drain- source voltage (V_{DS}) of 0.1V and 1 V is as shown in fig. 9. It is noted that a higher quantum capacitance/insulator capacitance can be reached at a gate voltage of 0.5 V and 0.9 V for a drain voltage of 0.1 V and 1 V beyond this voltages quantum capacitance/insulator capacitance gets decreased. Lower drain voltage shows significant capacitance effect.

F. Variation of Average Velocity with respect to Gate-Source Voltage (V_{GS})

The variation of average velocity with respect to gate-source voltage (V_{GS}) of CNTFET is as shown in fig. 10. It has been observed that the average velocity of carries increases with the increase in drain-source current beyond the threshold voltage. The average electron velocity at the top of the barrier increases with V_{DS} and then saturates. Saturating of velocity occurs in a ballistic transistor, but it occurs at the top of the barrier where the field is zero, rather than at the drain end where the field is high. The carrier velocity is expressed as

$$\langle v \rangle \equiv \frac{I_d(V_{GS}, V_{DS})}{Q(V_{GS}, V_{DS})}$$

Therefore average velocity of carrier at top of the barrier is defined as

$$\langle v(0) \rangle \equiv \frac{I_d(V_{GS}, V_{DS})}{-q\,[n^+(V_{GS}, V_{DS}) + n^-(V_{GS}, V_{DS})}$$

As observed from Fig. 10, the average velocity of carrier increases with gate-source voltage.

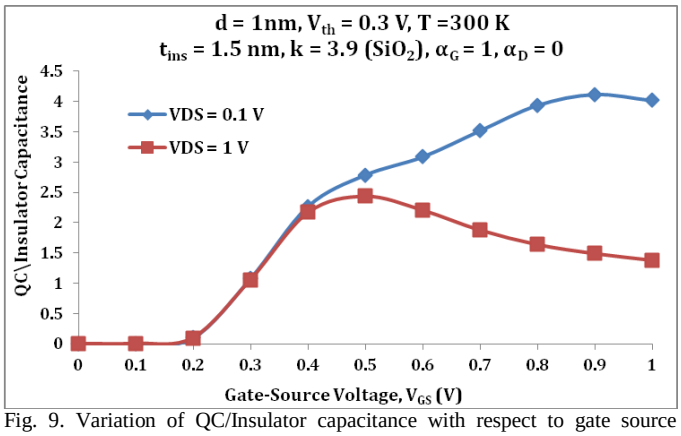

Fig. 9. Variation of QC/Insulator capacitance with respect to gate source voltage (V_{GS}) for a drain- source voltage (V_{DS}) of 0.1V and 1 V.

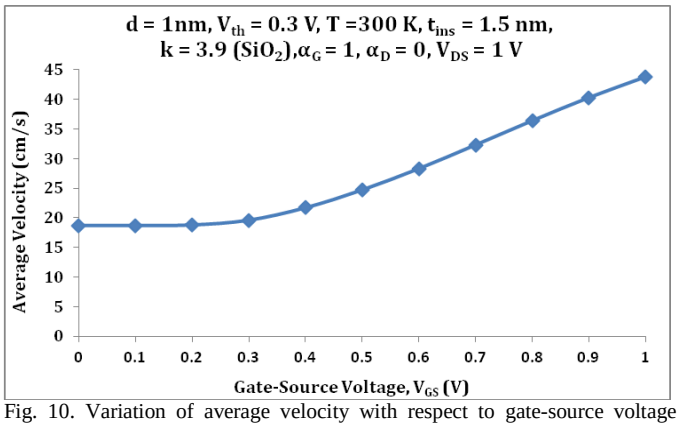

Fig. 10. Variation of average velocity with respect to gate-source voltage (*VGS*) of CNTFET.

Table 1. Comparison of Ballistic N-CNTFET with the 15nm N-MOSFET and 60nm Tri gate N-MOSFET.

Device Metrics	**15nm n-MOSFET [2]**	**60nm Tri gate n-MOSFET [2]**	**Ballistic n-CNTFET with CNT diameter = 1nm**
Ion	450 µA/µm	1140 µA/µm	33, 280 µA/µm
Ioff	180 nA/µm	70 nA/µm	37 nA/µm
Ion/Ioff	2500	16285.71	898730
SS	95 mV/decade	68 mV/decade	59.19 mV/decade
DIBL	100 mV/V	41 mV/V	0.60 mV/V

The comparison of n-type CNTFET with 15nm n-type MOSFET and 60nm Trigate n-type MOSFET is as shown in Table 1. It can be seen that the ballistic n-type CNTFET has high drive current (I_{on}), low leakage current (I_{off}), high I_{on}/I_{off} ratio i.e fast switching speed as compared to 15nm n-type MOSFET and 60nm Trigate n-type MOSFET. Also, the short-channel effects such as Subthreshold Slope (SS) and Drain Induced Barrier Lowering (DIBL) improves. Hence, we can say that the controllability of gate on the channel will be more in case of ballistic n-type CNTFET.

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V. CONCLUSIONS

It has been concluded that the ballistic CNTFET has high drive current (I_{on}), low leakage current (I_{off}), high I_{on}/I_{off} ratio i.e fast switching speed and improved short-channel effects such as Subthreshold Slope (SS) as well as Drain Induced Barrier Lowering (DIBL). Hence comparative device performance of CNTFET with 15nm N-MOSFET and 60nm Trigate MOSFET suggest that a CNTFET can be a successor to replace current Si MOSFET for various applications and Moore's Law will be extended well into the next decade.

ACKNOWLEDGMENT

One of the authors D. Dass gratefully acknowledges the University Grants Commission (U.G.C.), Govt. of India, for the award of 'Rajiv Gandhi National Fellowship' under the scheme funded by Ministry of Social Justice & Empowerment, Govt. of India.

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