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Fabrication and Characterization of Ti-Pt/HfO_2/SiO_2~4.5nm/n-Si Nanoscale Device for Advanced CMOS Applications

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***Abstract*—**Downscaling is one of the attractive features supporting the technology node of present era. Ensuring the current status of ITRS, we reported the fabrication of nano-scale device based on high-k dielectric HfO_2. To examine the interfacial and structural properties of the grown films, various diagnostic techniques including Ellipsometry measurements, Atomic force microscopy (AFM), Field Emission Scanning Electron Microscopy (FESEM) and Fourier Transform Spectroscopy (FT-IR) were taken into account. Investigation of the electrical behavior of thin films directly corresponds to Capacitance-Voltage (C-V), Conductance-Voltage (G-V) and Current density versus Voltage (J-V) measurements. The fabricated nano-MOS offered the improved performance in terms of its reduced equivalent oxide thickness (EOT~3.87), leakage current density ($J = 6.5 \times 10^{-8}$ A/cm^2 at $V_g = 1V$) and Interface trap density ($D_{it} = 0.436 \times 10^{13}$ eV^{-1}cm^{-2}). Smaller EOT combined with the smaller leakage current can unlock the doors of power saving for nano-scale devices.

***Keywords*—** High-k dielectrics; ALD; MOScap; interfacial layer; FTIR; D_{it}; EOT.

I. INTRODUCTION

As the thickness of SiO_2 gate dielectric films used in CMOS devices is shrinked below 1.5 nm, the gate leakage current level becomes quite objectionable [1-3]. Extensive efforts have been made for finding the alternative gate dielectrics to triumph over the problem of leakage current [4-6]. Insulating materials with large dielectric constants (named as high-k materials) are alluring the modern industry owing to their potential use as gate dielectrics in metal-oxide semiconductor field-effect transistor (MOSFETs) [7-11]. Leakage current of gate oxides can be suppressed by the introduction of high-k dielectric to real applications [12-14]. A number of high-k dielectrics that have been dynamically pursued to replace SiO_2. Among them are cerium oxide CeO_2 [15], gadolinium oxide Gd_2O_3 [16], neodymium oxide Nd_2O_3 [17], aluminum oxide Al_2O_3 [18], lanthanum aluminum oxide $LaAlO_3$ [19], tantalum pentoxide Ta_2O_5 [20], titanium dioxide TiO_2 [21], zirconium dioxide ZrO_2 [22], HfO_2-CexHf1-xO_2 [23], hafnium silicate HfSixOy [24], and rare-earth scandates $GdScO_3$ [25], and $SmScO_3$ [26]. High-k materials hold the promise of achieving very high capacitance densities with relatively thicker films. However, finding a suitable high-k material is a major challenge. It appears that, after investigating a whole host of materials, Hafnium based gate dielectrics have emerged as the "ultimate" choice for high-k materials. The ideal motivation for moving to high-k gate dielectric was the need to trim down direct tunneling leakage currents [27]. Direct deposition of HfO_2 on Si substrate induces defects [28] due to biased amorphicity and residual contamination. This defect leads to high breakdown fields and avoids reduction of FET channel mobility [29]. A number of concerns are related with high-k dielectrics, which includes Coulomb scattering from bulk oxide charges, surface roughness scattering, interface fixed charges, dielectric charge trapping and remote phonon scattering associated with reliability problems. A peep into the past research reveals following issues to be taken into consideration:

- Influence of manufacturable ex situ and in situ high-k dielectrics
- Conventional process routes and materials such as HfO_2, ZrO_2, Al_2O_3 to form quality gate stacks
- Engineering the high-k channel interface by valuation of bi-layer schemes to attain low Dit and thin EOT.
- Development of various schemes or models for passivating these defects.

We have worked on several issues related to direct deposition of HfO_2 on Si substrate. The problems arised has been resolved by incorporating good quality SiO_2 as an interfacial layer.

II. EXPERIMENTAL DETAILS

The fabricated double layer nano-MOS is shown in Figure 1. Single side polished (SSP) n-type Si <100> substrates having a resistivity of 1-5 Ω cm were chemically cleaned by the standard RCA method. SiO_2 ~ 4.5nm was grown using RTP at 900 ^{0}C having 900 sccm O_2 flow per minute under atmospheric conditions. Atomic layer deposition (ALD) technique was used to deposit 10nm thin hafnia film on silicon dioxide at 200^{0}C by thermal method. The physical thickness of SiO_2 and HfO_2 films were determined by using SE800 Ellipsometer. For the top gate electrode, 1000^{0}A thick layer with Ti = 20nm and Pt = 60nm was deposited by 4 target E-beam evaporator system over a circular area of 2.2×10^{-4} cm^2 through a shadow mask. To remove the native oxide on the back side, etching was performed by buffered hydrofluoric acid (BHF) followed by rinsing in de-ionized water. On the back side of silicon wafer, Aluminum film was deposited for

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making back contact. Finally, Post metallization annealing (PMA) was performed at 420 °C for 20 minutes using forming gas (96%N_2, 4%H_2) ambient. To extract the various performance parameters, the measurements of the fabricated device were carried out using Keithley 4200-SCS at room temperature under dark conditions. The process flow of the fabricated device can be clearly illustrated as:

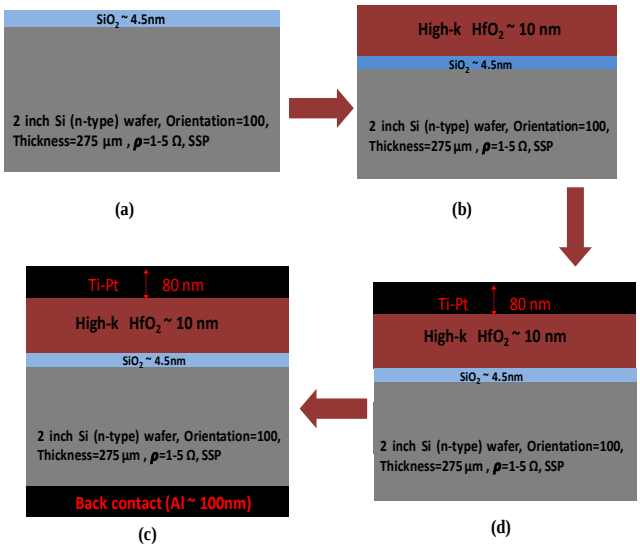


Fig. 1. Process flow for fabricated nano-scale device (a) SiO_2 interfacial layer growth (b) ALD HfO_2 ~ 10nm (c) Ti-Pt front gate deposition and (d) Al as a back contact.

III. AFM Study

Using AFM, it is quite viable to evaluate the roughness of a sample surface at a high resolution. Moreover, this method distinguishes the sample based on its mechanical properties such as - hardness and roughness.

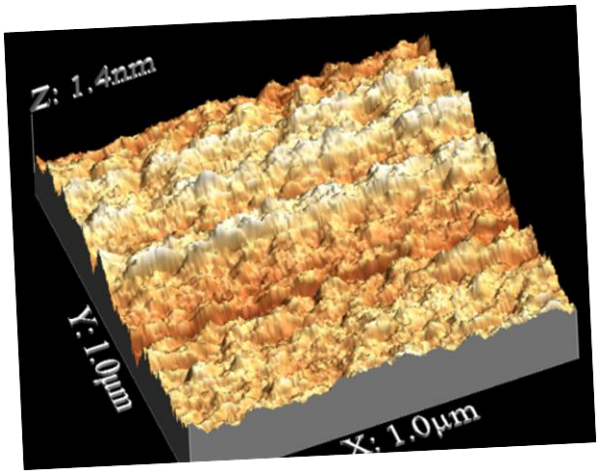


Fig. 2. 3-D AFM image of SiO_2 having 2 × 2 µm scanning area.

Figure 2 and 3 represents the atomic force measurement of silicon dioxide and hafnia films respectively. The surface roughness for SiO_2 film was found to be 0.1838nm while the hafnia film prepared by atomic layer deposition technique indicates the rms value of 0.007295 nm.

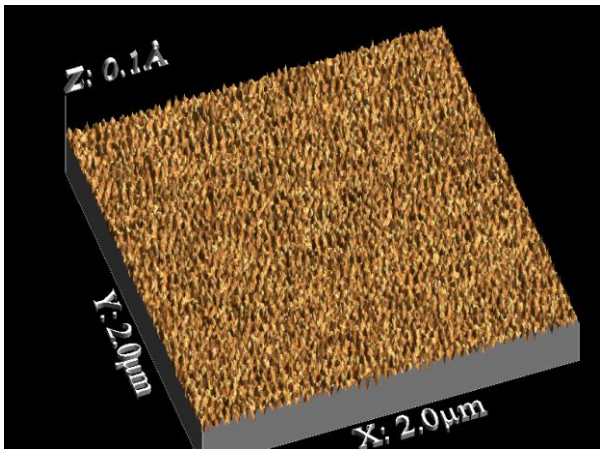


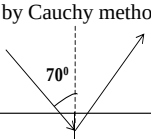
Fig. 3. 3-D AFM image of HfO_2 having 2 × 2 µm scanning area.

The reduced roughness of SiO_2 film was the result of effective rapid thermal processing. In principle, the morphology of hafnia film exhibited the excellent film quality.

IV. Ellipsometry Measurements

Ellipsometry works on the principle of interaction of light with the sample which produces a change in the intensity/polarization of the measuring beam. The change contains the information on sample which is measured. In this letter, we have used the Cauchy model for thickness and refractive index measurements. Cauchy method reflects the relationship existing between refractive index 'η' and wavelength 'λ' of a light for a transparent material. The measured parameters from this method can be represented by Table 1 as:

Table 1. Measured parameters by Cauchy method.



Air	η_{Air}
Cauchy HfO_2	2.21
Cauchy SiO_2	1.45
	η = 3.66, K = 0.027

Here, the incident angle was kept as 70^0C and computed extinction coefficient 'K' was 0.027. The respective measured thickness of SiO_2 and HfO_2 was 4.5nm and 10nm while their refractive indexes were found to be 2.21 and 1.45 respectively.

V. FESEM Analysis

Figure 4 represents the field emission scanning electron microscopy analysis to corroborate the thickness of the interfacial layer. By using this physical characterization, we are certain to display the thickness of the grown SiO_2 film ~ 4.5nm. Prior to the growth of interfacial layer, standard RCA

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cleaning process was performed to remove the native oxides and impurities.

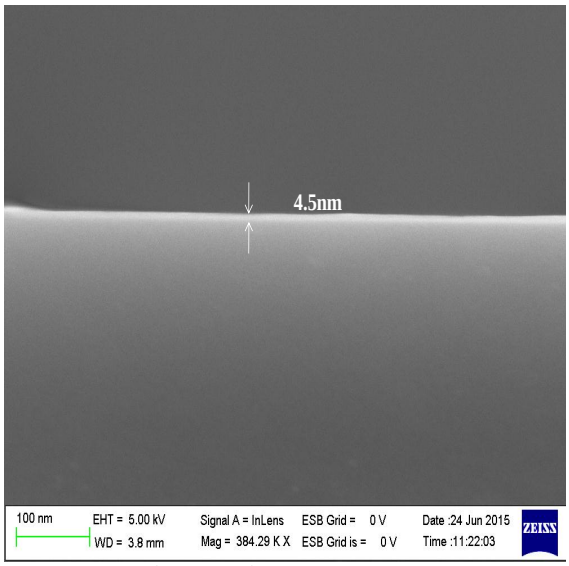

Fig. 4. FESEM image of SiO_2 interfacial layer (Cross-sectional view).

The cross-sectional FESEM analysis reveals the formation of defect-free interfacial layer growth.

VI. FT-IR Characterization

Figure 5 represents the FT-IR spectra of the hafnia film. The bonding structure was investigated by finding oxygen content in the film. To reflect the absorbance of the grown film, infrared absorption spectra of the bare-Silicon wafer was used as background spectra and finally subtracted from the total spectrum.

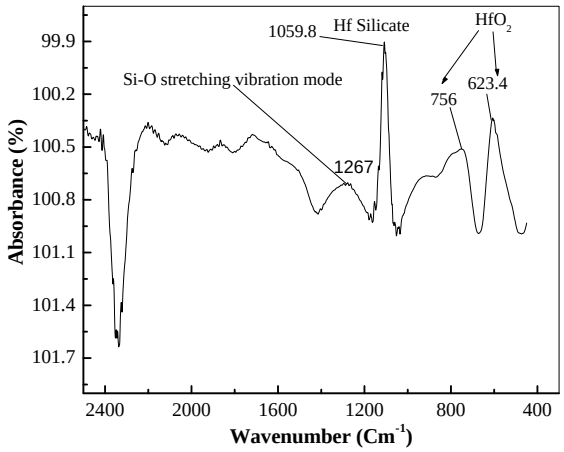

Fig. 5. FT-IR analysis of ALD Hafnia film.

The sharp vibration bands observed in the range of 623-756 cm^{-1} validates the presence of HfO_2 (Frank, et al. 2004). The peak at 1059 cm^{-1} corresponds to the shifting peak position of Hf-O towards the higher wave number series, and is somewhat following the crystalline category.

VII. Results And Discussion

In this section, we shall deal with the electrical characterization namely C-V, G-V and I-V of the fabricated device structure.

A. Capacitance Versus Voltage (C-V)

Figure 6 shows the Capacitance-voltage characteristics of Ti-Pt/HfO_2/SiO_2/Si MOS capacitor. C-V curve measurements were performed for frequency variation from 1 KHz and 1 MHz. However, all the calculations were carried out at high-frequency 500 KHz. The dielectric constant (K) of the device was calculated to be 14.6 as extracted from the accumulation region of C-V curve and the Equation (1) was used for its computation as:

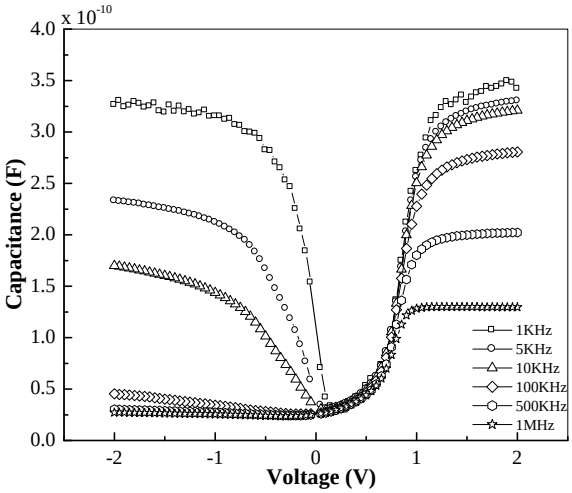

Fig. 6. C-V characterization of Ti-Pt/HfO_2/SiO_2/n-Si of nano-scale MOS.

$$K = \frac{(C_{ox} t_{ox})}{\epsilon_0 A} \quad (1)$$

where, C_{ox} = oxide capacitance, t_{ox} = oxide thickness, ϵ_0 = permittivity of the free space and 'A' represents the electrode area.

The effective oxide charge (Q_{eff}) was calculated using Equation (2) as:

$$Q_{eff} = (\Delta V_{fb} \times C_{ox}) / (q \times A) \quad (2)$$

where, ΔV_{fb} = flat band voltage shift, C_{ox} = Oxide Capacitance and 'q' denotes the electronic charge.

The value of Q_{eff} for 500 KHz was found to be 0.4545×10^{15} cm^{-2}. A sufficient positive shift occurred in the flat-band voltage because of the existence of negative trap charges in the fabricated p-MOS structure.

B. Conductance Versus Voltage (G-V)

Figure 7 shows G-V characteristics of the Ti-Pt/HfO_2/SiO_2/n-Si stack studied at a frequency of 100 KHz and 500 KHz. The measurements demonstrate that there is an increase in the conductance value i.e. G_{max} at 500 KHz near the flat band voltage regime.

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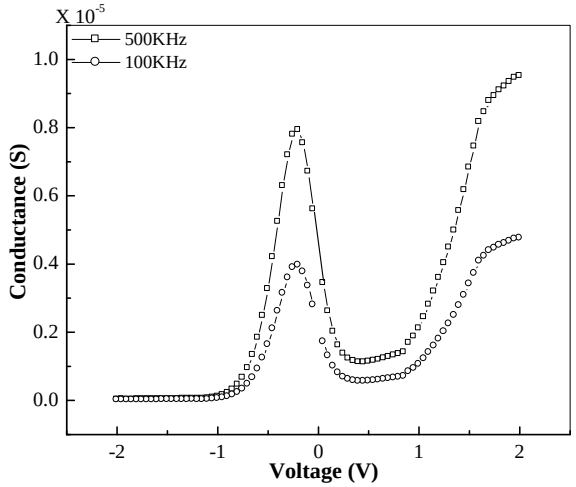

Fig. 7. G-V characterization of Ti-Pt/HfO_2/SiO_2/n-Si of nano-scale MOS.

The interface trap density (D_{it}) at interface was calculated from the Conductance Voltage characteristics by the following formula [8].

$$D_{it} = \frac{2\omega C_{ox}^{2} G_{max}}{qA\left[G_{max}^{2} + \omega^{2}(C_{ox} - C_m G_{max})^2\right]} \quad (3)$$

where, C_m is maximum capacitance, G_{max} is the maximum conductance and ω is frequency. The obtained D_{it} value for the fabricated capacitor was found to be 0.436×10^{13} eV^{-1} cm^{-2} as per the above given relation. The reduction in the interface trap density D_{it} is the outcome of improved dangling bonds at the interface.

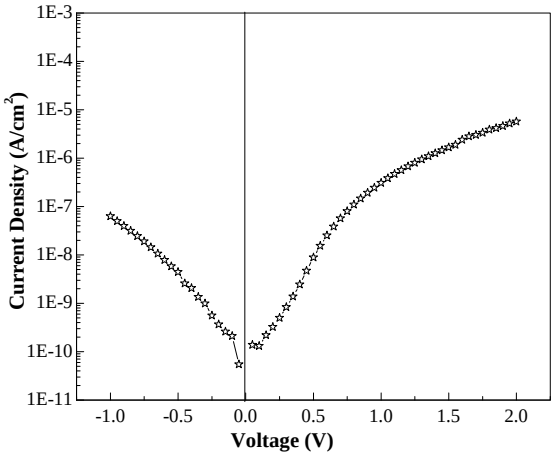

Fig. 8. J-V curve of Ti-Pt/HfO_2/SiO_2/n-Si MOS capacitor.

C. Current Density Versus Voltage (J-V)

The leakage current density (J) of Ti-Pt/HfO_2/SiO_2/n-Si stack was measured as a function of voltage as represented by Figure 8. The leakage current density was observed to be improved up to 6.5×10^{-8} A/cm^2 after the incorporation of good quality interfacial layer of SiO_2 owing to the reduction of defects at the interface of Si/HfO_2 stack. Consequently, the significant decline in the device leakage was the result of injection of charge carriers into the conduction band of hafnia film by Fowler-Northeium (FN) tunneling. This leakage reduction accounts for the enhanced device performance.

VIII. CONCLUSIONS

We successfully fabricated Ti-Pt/HfO_2/SiO_2~4.5nm/n-Si nanoscale device with achieved K~14.6. AFM studies confirms that the smoothness of grown films. A remarkable decrease in the interface trap density was observed owing to the interface improvement of Si/SiO_2/HfO_2 stack. Moreover, effective reduction in EOT was achieved. High-k deposition along with the ultra thin interfacial layer of SiO_2 will leads to further device scaling without adverse leakage effects. Such a progress in device scaling is the gateway to power saving.

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