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Variation in Dc Characteristics of Digital Gates Using Floating-Gate MOSFET

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***Abstract*—**In this paper, the design of XOR and XNOR gates using floating-gate MOSFET (FGMOS) has been presented. The performance of XOR and XNOR gates implemented using FGMOS has been compared with their CMOS versions. It has been observed that by varying the bias voltage of FGMOS, the dc characteristics of XOR and XNOR gates can be varied that result in less switching threshold voltage and increased noise margins. The performance of these circuits has been ascertained by PSpice simulations carried out using level 7 parameters in 0.13 μm technology with a supply voltage of 1V.

***Keywords*—** CMOS; FGMOS; dc characteristics; switching threshold voltage; noise margin.

I. INTRODUCTION

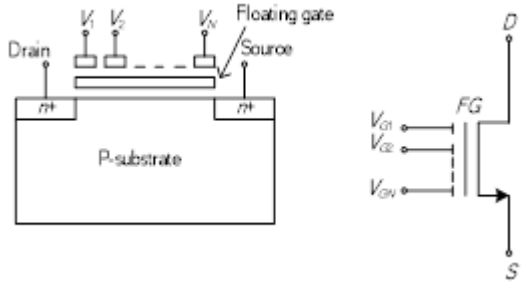
The advancement in VLSI technology combined with the increased market demands to develop small sized and efficient portable devices have increased the interest in designing circuits at low voltage supply and low power consumption. The operation of VLSI circuits in low power regime is one of the major requirements for modern portable electronic gadgets [1], [2]. There are many challenges for mixed signal design to be adaptable for system on chip implementation. The major considerations in designing these mixed signal circuits are high speed, low voltage and low power operation. It is also necessary to improve the noise immunity of digital circuits for reliable operation of VLSI chips [3], [4]. In this paper we have employed Floating-gate MOS transistor (FGMOS) for designing XOR and XNOR gates and compared its performance with their CMOS versions. The performance of these circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 μm CMOS technology with supply voltage of 1V.

II. FLOATING-GATE MOS TRANSISTOR

Floating-Gate MOS transistor (FGMOS) is a kind of transistor in which its driving terminal is electrically isolated from the rest of device. The structure of floating-gate MOSFET (FGMOS) is similar to a conventional MOSFET expect that its multiple input gates are capacitively connected to the conventional gate which becomes floating being embedded in insulator. This device has same drain, source and bulk terminals besides a number of input terminals. The conventional gate (floating-gate) is not accessible anymore for signal application rather it is controlled indirectly through capacitance coupling by applying signals at control gates [4-6]. The cross-sectional view and symbol of a typical n-channel, n-inputs FGMOS transistor is shown in Fig. 1.

III. XOR GATE

The XOR circuit is basic building block in various circuits, especially arithmetic circuits such as adders and multipliers, compressors, comparators, parity checkers, code converters, error-detecting or error-correcting codes and phase detectors [7]. The *XOR* (*exclusive-OR*) *gate* acts in the same way as the logical "either/or". In XOR gate, the output is high only if either, but not both of the inputs are one and the output is low if both inputs are one or if both inputs are zero i.e. the output becomes high if the inputs are different and low if the inputs are same. The circuit for CMOS XOR gate is shown in Fig. 2.



(a) Structure (b) Symbol

Fig. 1. Structure and symbol of n-channel FGMOS.

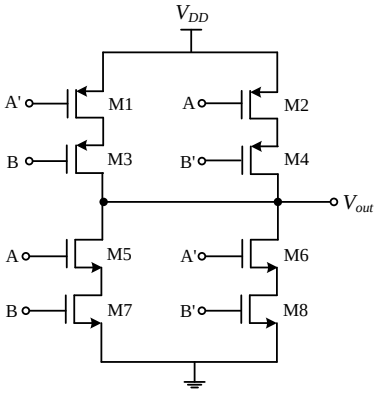


Fig. 2. XOR gate.

The performance of XOR gate can be characterized through its dc response which has been obtained by simulating

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the circuit of Fig. 2 by selecting *W/L* of P-channel MOSFETs as 26µm/0.13µm and N-channel MOSFETs as 13µm/0.13µm with the supply voltage of 1V and are shown in Fig 3. From these characteristics we have calculated parameters like switching threshold voltage and noise margin to ascertain the performance of these circuits. The switching threshold voltage (V_S) is defined as the input voltage that gives an identical output voltage. V_S can be obtained graphically at the intersection of the VTC curve and the line given by $V_{out} = V_{in}$ [8, 9]. The voltage noise margins can be obtained as $NM_H = V_{OH} - V_S$ and $NM_L = V_{OL} - V_S$.

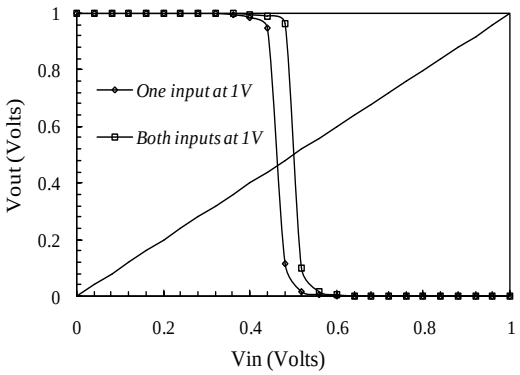

Fig. 3. Dc characteristics of XOR gate.

The presence of two independent inputs implies that more than one dc curve is needed to describe the circuit behavior. Since there are two inputs, the actual characteristics depend on how the inputs are switched. We first consider the case when one input is held high and other is switched from low to high. A second case exists when both inputs are connected together and switched from low to high. These two possibilities lead to the two distinct transitions and are shown in the dc characteristics curve [10], [11].

Case I: When one input is tied and other is switched from 0 V to 1 V. Then, from Fig. 3 switching threshold voltage (V_S), high and low noise margins are obtained as follows: V_S = 0.46 V, NM_H = 0.54 V and NM_L = 0.46 V.

Case II: When both inputs are tied together and switched from 0 V to 1 V. Then, from the Fig. 3, switching threshold voltage (V_S), high and low noise margins are obtained as follows:
V_S = 0.5 V, NM_H = 0.5 V and NM_L = 0.5 V.

IV. FGMOS BASED XOR GATE

In order to enhance the performance of XOR gate in terms of switching threshold voltage and noise margin, the circuit of XOR gate has been implemented using FGMOS as shown in Fig. 4. The dc characteristics of XOR gate using FGMOS has been obtained at different values of bias voltages by selecting *W/L* of P-channel MOSFETs as 26µm/0.13µm and N-channel MOSFETs as 13µm/0.13µm with the supply voltage of 1V and are shown in Figs. 5 and 6 respectively. In Fig. 5, V_{bn} is kept fixed at 1 V and V_{bp} is varied from 0 V to 1 V. Similarly in Fig. 6, V_{bn} is varied from 0 V to 1 V while keeping V_{bp} constant at 0 V.

From Figs. 5 and 6, we have calculated the switching threshold voltage (V_S) and noise margins NM_H and NM_L at different values of V_{bp} and V_{bn} as shown in Table I and II respectively.

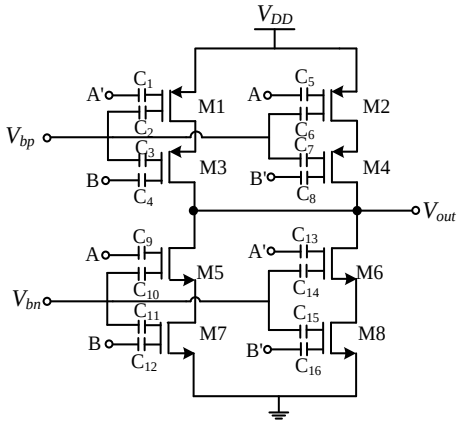

Fig. 4. FGMOS XOR gate.

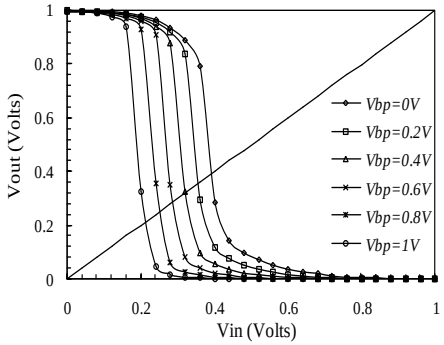

Fig. 5. Dc characteristics of FGMOS XOR at different V_{bp}.

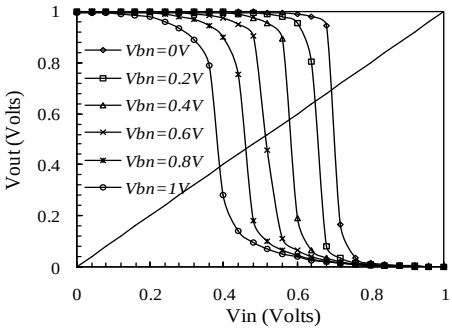

Fig. 6. Dc characteristics of FGMOS XOR at different V_{bn}.

Table I. Noise margins of FGMOS XOR at different V_{bp}.

V_{bp} (Volts)	V_S (Volts)	NM_H (Volts)	NM_L (Volts)
0	0.38	0.62	0.38
0.2	0.35	0.65	0.35
0.4	0.32	0.68	0.32
0.6	0.28	0.72	0.28
0.8	0.24	0.76	0.24
1	0.20	0.80	0.20

As shown in table I, when bias voltage of p-channel FGMOS (V_{bp}) is varied from 0 V to 1 V at constant bias

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voltage of n-channel FGMOS (V_{bn} = 1V), the switching threshold voltage (V_S) and low noise margin (NM_L) of FGMOS inverter decreases from 0.38 V to 0.20 V but high noise margin (NM_H) increases from 0.62 V to 0.80 V. Similarly in table II, decreasing bias voltage of n-channel FGMOS (V_{bn}) from 1 V to 0 V, keeping V_{bp} fixed at 0 V increases NM_L from 0.38 V to 0.70 V. Thus, we observe that NM_L is maximum when $V_{bp} = V_{bn} = 0$ V and NM_H is maximum when $V_{bp} = V_{bn} = 1$ V.

Table II. Noise margins of FGMOS XOR at different V_{bn}.

V_{bn} (Volts)	V_S (Volts)	NM_H (Volts)	NM_L (Volts)
0	0.70	0.30	0.70
0.2	0.64	0.36	0.64
0.4	0.58	0.42	0.58
0.6	0.51	0.49	0.51
0.8	0.45	0.55	0.45
1	0.38	0.62	0.38

V. XNOR GATE

The *XNOR (exclusive-NOR)* gate is a combination of XOR gate followed by an inverter as shown in Fig. 7. In XNOR gate, the output is low if either, but not both of the inputs are one and the output is high only if both inputs are one or if both inputs are zero i.e. the output becomes low if the inputs are different and high if the inputs are same.

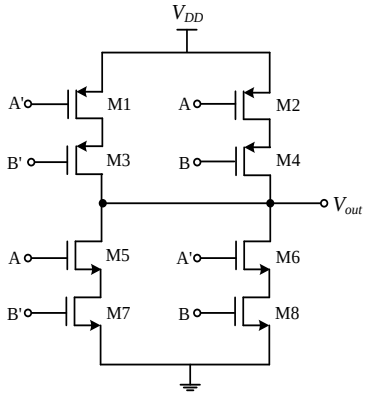

Fig. 7. XNOR gate.

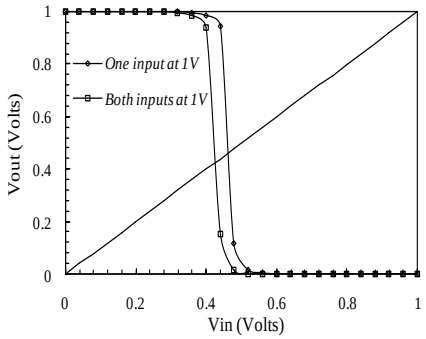

Fig. 8. Dc characteristics of XNOR gate.

The circuit of Fig. 7 has been simulated to obtain its dc characteristic curves as shown in Fig. 8.

Case I: When one input is tied and other is switched from 0 V to 1 V. Then, from Fig. 8 switching threshold voltage (V_S), high and low noise margins are obtained as follows:
V_S = 0.46 V, NM_H = 0.54 V and NM_L = 0.46 V.
Case II: When both inputs are tied together and switched from 0 V to 1 V. Then, from the Fig. 8, switching threshold voltage (V_S), high and low noise margins are obtained as follows:
V_S = 0.42 V, NM_H = 0.58 V and NM_L = 0.42 V.

VI. FGMOS BASED XNOR GATE

Similarly, the circuit of XNOR gate is implemented using FGMOS as shown in Fig. 9.

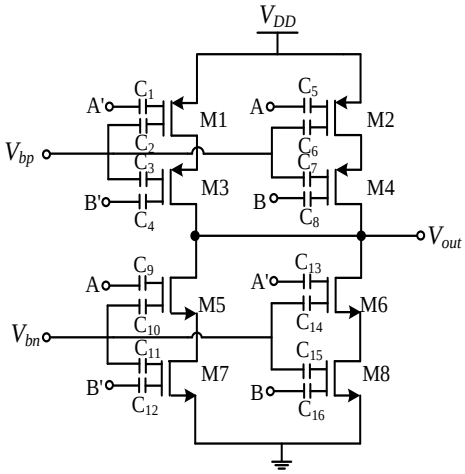

Fig. 9. FGMOS XNOR gate.

The circuit of FGMOS XNOR gate has been simulated to obtain dc characteristics by selecting *W/L* of p-channel MOSFETs as 26µm/0.13µm and n-channel MOSFETs as 13µm/0.13µm with the supply voltage of 1V and is shown in Figs. 10 and 11 respectively. In Fig. 10, bias voltage of p-channel FGMOS transistors (V_{bp}) is varied from 0 V to 1 V, while keeping bias voltage of n-channel FGMOS transistors (V_{bn}) fixed at 1 V. Similarly in Fig. 11, V_{bn} is varied from 0 V to 1 V, while keeping V_{bp} fixed at 0 V.

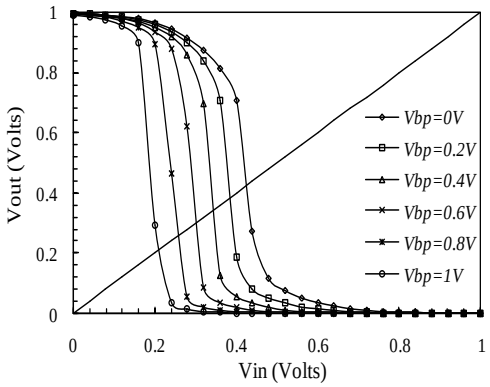

Fig. 10. Dc characteristics of FGMOS XNOR at different V_{bp}.

From Figs. 10 and 11, we have calculated the switching threshold voltage (V_S) and noise margins NM_H and NM_L at

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different values of V_{bp} and V_{bn} as shown in Table III and IV respectively.

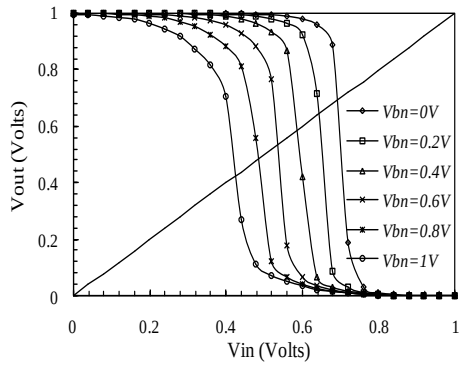

Fig. 11. Dc characteristics of FGMOS XNOR at different V_{bn}.

Table III. Noise margins of FGMOS XNOR at different V_{bp}

V_{bp} (Volts)	V_S (Volts)	NM_H (Volts)	NM_L (Volts)
0	0.42	0.58	0.42
0.2	0.38	0.62	0.38
0.4	0.34	0.66	0.34
0.6	0.29	0.71	0.29
0.8	0.25	0.75	0.25
1	0.20	0.80	0.20

Table IV. Noise margins of FGMOS XNOR at different V_{bn}

V_{bn} (Volts)	V_S (Volts)	NM_H (Volts)	NM_L (Volts)
0	0.69	0.31	0.69
0.2	0.64	0.36	0.64
0.4	0.59	0.41	0.59
0.6	0.53	0.47	0.53
0.8	0.48	0.52	0.48
1	0.42	0.58	0.42

As shown in table III, when bias voltage of p-channel FGMOS (V_{bp}) is varied from 0 V to 1 V at constant bias voltage of n-channel FGMOS (V_{bn} = 1V), the switching threshold voltage (V_S) and low noise margin (NM_L) of FGMOS inverter decreases from 0.42 V to 0.20 V but high noise margin (NM_H) increases from 0.58 V to 0.80 V. Similarly in table IV, decreasing bias voltage of n-channel FGMOS (V_{bn}) from 1 V to 0 V, keeping V_{bp} fixed at 0 V increases NM_L from 0.42 V to 0.69 V. Thus, NM_L is maximum i.e., 0.69 V when $V_{bp} = V_{bn} = 0$ V and NM_H is maximum i.e., 0.80 V when $V_{bp} = V_{bn} = 1$ V.

VII. Conclusion

The design of XOR and XNOR gates using FGMOS has been presented in this paper. A comparative study of these gates with regard to its voltage transfer characteristics has also been carried out. We have found that by varying the bias voltage of FGMOS, the voltage transfer characteristics of inverter can be modified resulting in increased noise margins as compared to its CMOS versions. The performance of these circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 µm CMOS technology with a supply voltage of 1 V.

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