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Comparative Study of CMOS and FGMOS based Digital Gates

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Abstract— The portability and low power consumption of modern electronic gadgets have aroused great interest in the design of low voltage circuits. Such applications also demand low power dissipating circuits for longer life and smaller weight of implantable products. The ultimate goal is to have battery less system as battery forms a significant part of weight and volume of the system. As the device channel length is scaled down into submicron regime and the gate oxide thickness reduces to only several nanometers, the supply voltage is required to be reduced in order to ensure device reliability. However, the reduction in supply voltage has its own limitation due to the presence of threshold voltage of MOS transistor which limits the supply voltage to be equal to or greater than threshold voltage. Therefore, conventional CMOS technique for circuit realization is no more of use for low-power circuit realization. Literature survey reveals a number of interesting applications that have been exploited for the reduction of threshold voltage in VLSI circuits. Floating-gate MOSFET (FGMOS) has been widely employed for designing low voltage and low power digital circuits. FGMOS is a special type of MOS transistor with multiple input gates and a unique feature of threshold voltage tunability. As a consequence, the characteristics of FGMOS based circuits can be altered by varying the threshold voltage using a bias voltage and hence provides tunability to the circuit. This paper presents the comparison of various digital circuits using CMOS and FGMOS. It has been observed that variation of bias voltage in FGMOS reduces the propagation delay and energy delay product of digital circuits and hence enhances the operating speed. The performance of these circuits has been ascertained by PSpice using level 7 parameters in 0.13 µm CMOS technology with supply voltage of 1 V.

Keywords— CMOS; FGMOS; propagation delay; energy delay product.

I. INTRODUCTION

The growing demand of high performance integrated circuits (ICs) has resulted in faster switching speed, increased number of transistors, higher functional density and larger chip size. The continuous increase in device integration is responsible for the density, speed and growth of modern electronic systems. The operation of VLSI circuits in low power regime is one of the major requirements for modern portable electronic gadgets [1], [2]. There are many challenges for mixed signal design to be adaptable for system on chip implementation. The major considerations in designing these mixed signal circuits are high speed, low voltage and low power operation. It is also necessary to improve the noise immunity of digital circuits for reliable operation of VLSI chips. CMOS circuits are widely used in digital integrated circuits due to their high performance [3]. The design of CMOS digital circuits with very low power consumption and without much degradation in speed has always been the focal point of circuit designers particularly in sub-micron regime. Since, there is always a trade-off between power dissipation and time delay in digital circuits, therefore reducing the power dissipation and still maintaining the performance of circuits is very much desirable in digital designs. With the immense demand for portable and battery driven applications, there is a need for new circuit design techniques to implement high performance and low power digital circuits. Further, with reducing feature size of devices, the lowering of operating supply voltage is obvious but at the expense of speed. Hence, for optimum performance of digital circuits, alternative mechanism should be explored [4], [5]. In this paper, we have employed floating-gate MOSFET (FGMOS) to enhance the performance parameters of digital gates and compared its performance with its conventional CMOS counterpart. The performance of these circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 µm CMOS technology with a supply voltage of 1 V.

II. FLOATING-GATE MOS TRANSISTOR

Floating-Gate MOS transistor (FGMOS) is basically a modified form of simple MOSFET where extra capacitances have been introduced between the conventional gate and the multi-input signal gates. By applying a bias voltage on one of the input gates, the threshold voltage of FGMOS can be changed. The equivalent schematic for an N-input n-channel FGMOS is shown in Fig. 1.

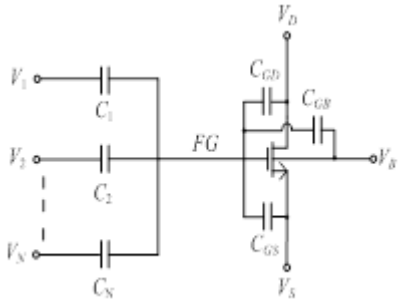

Fig. 1. Floating-gate MOSFET.

A number of secondary gates or inputs are deposited above the floating-gate (FG) which are electrically isolated from it and are only capacitively connected to FG. Since FG is

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completely surrounded by highly resistive material, so for dc operation, FG acts as floating node. Programming of the FGMOS introduces a charge on its floating-gate that shifts the threshold voltage and thus, provides a control over the device functionality [6, 7].

III. Design of Digital Gates using FGMOS

The circuit of FGMOS inverter is shown in Fig. 2. The circuit is similar to that of CMOS inverter [8-11] except that coupling capacitances are introduced between conventional gate and the multi-input signal gates. The bias voltages V_{bp} and V_{bn} provide tunability to the threshold voltages of M1 and M2 respectively. It is, therefore, expected that by varying the bias voltages, the threshold voltage of the FGMOS inverter can be changed.

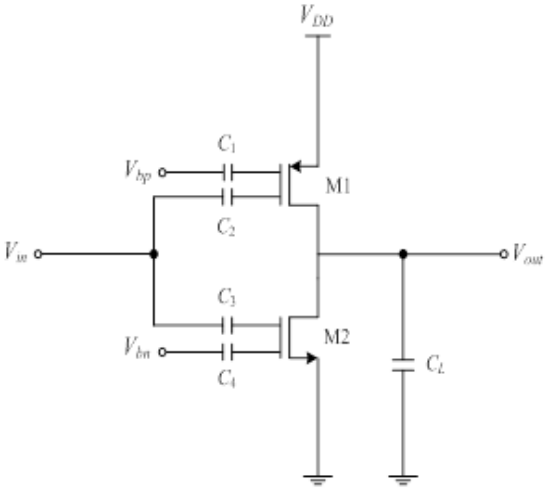

Fig. 2. FGMOS inverter.

The circuit of Fig. 2 has been simulated to obtain transient response by selecting *W/L* of M1 as 26 µm/0.13 µm and M2 as 13 µm/0.13 µm with a supply voltage of 1 V. It has been found that pulse response in FGMOS inverter can be varied with bias voltage resulting in different values of propagation delay as shown in Figs. 3 and 4 respectively.

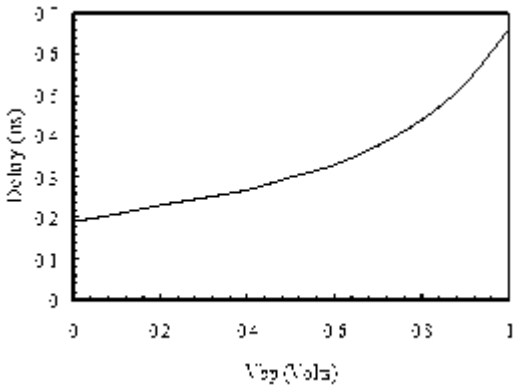

Fig. 3 .Propagation delay at different V_{bp}.

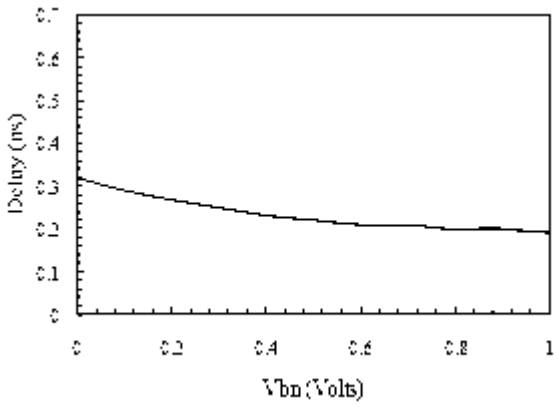

Fig. 4. Propagation delay at different V_{bn}.

The propagation delay at different values of V_{bp} and V_{bn} is shown in Table I.

TABLE I Effect of bias voltage on propagation delay.

V_{bp} (V)	Delay (ns)	V_{bn} (V)	Delay (ns)	
0	0.19	0	0.32	
0.1	0.21	0.1	0.29	
0.2	0.23	0.2	0.27	
0.3	0.25	0.3	0.25	
0.4	0.27	0.4	0.23	
0.5	0.30	0.5	0.22	
0.6	0.33	0.6	0.21	
0.7	0.38	0.7	0.21	
0.8	0.44	0.8	0.20	
0.9	0.53	0.9	0.20	
1	0.66	1	0.19	

From the above table, it has been observed that in FGMOS inverter if bias voltage of p-channel FGMOS transistor is increased from 0V to 1V keeping bias voltage of n-channel FGMOS fixed at 1V, the propagation delay increases from 0.19 ns to 0.66 ns. Similarly if bias voltage of n-channel FGMOS is increased from 0 V to 1 V keeping bias voltage of p-channel FGMOS fixed at 0 V, the propagation delay decreases from 0.32 ns to 0.19 ns. Therefore, the appropriate selection of bias voltages of n and p-channel FGMOS at 1V and 0V respectively decreases the propagation delay of FGMOS inverter, thus enhancing the operating speed.

Now, the values of propagation delay obtained from the transient characteristics have been used to calculate the energy delay product (EDP) at different values of supply voltage (V_{DD}) as shown in table 2. EDP represents the trade-off between power dissipation and the speed, implying the operation of digital circuits at low power would result in loss of speed. Therefore, lower value of energy delay product is required for circuits suitable for operation with low operating voltage and low power consumption.

The results obtained from the above table show that EDP is a function of supply voltage and for V_{DD} = 1 V, FGMOS inverter has EDP = 1×10^{-23} Js where as the value of EDP for CMOS inverter is 2×10^{-23} Js.

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TABLE II. EDPs of CMOS and FGMOS inverter.

V_{DD} (Volts)	CMOS	FGMOS
	EDP (Js)	EDP (Js)
0.1	0.02×10^{-23}	0.01×10^{-23}
0.2	0.08×10^{-23}	0.04×10^{-23}
0.3	0.18×10^{-23}	0.09×10^{-23}
0.4	0.32×10^{-23}	0.16×10^{-23}
0.5	0.5×10^{-23}	0.25×10^{-23}
0.6	0.72×10^{-23}	0.36×10^{-23}
0.7	0.98×10^{-23}	0.49×10^{-23}
0.8	1.28×10^{-23}	0.64×10^{-23}
0.9	1.62×10^{-23}	0.81×10^{-23}
1	2×10^{-23}	1×10^{-23}

The transient characteristics of other digital gates such as NAND and NOR gates using FGMOS has also been obtained using PSpice in 0.13 µm CMOS technology. From the simulation results, it has been observed that the propagation delay and EDP parameter for FGMOS based NAND gate is less (t_p = 0.18ns and EDP = 0.9×10^{-23}Js) as compared to CMOS NAND gate which has (t_p = 0.28ns and EDP = 1.4×10^{-23}Js). Similarly, NOR gate using FGMOS has lower values of t_p and EDP i.e. 0.24ns and 1.2×10^{-23}Js followed by CMOS having t_p = 0.42ns and EDP = 2.1×10^{-23}Js . Therefore, FGMOS based digital gates provide better operating speed at less power consumption as compared to CMOS.

IV. Conclusion

In this paper, we have presented the design of digital gates using FGMOS. A comparative study of CMOS and FGMOS based inverter and universal gates with regard to propagation delay and energy delay product has been carried out. We have found that by varying the bias voltage of FGMOS, propagation delay and energy delay product can be reduced in FGMOS. Therefore, FGMOS can be used as an alternate for designing high speed and low power digital circuits. The functionality of these circuits has been verified through PSpice simulations carried out using level 7 parameters in 0.13 µm CMOS technology with a supply voltage of 1 V.

References

[1] R. Gonzalez, B. M. Gordon and M. A. Horowitz, "Supply and threshold voltage scaling for low power CMOS," IEEE J. Solid-State Circuits, vol. 32, no. 8, pp. 1210-1216, Aug. 1997.
[2] E. Sanchez-Sinencio and A. G. Andreou, Low-Voltage/Low-Power Integrated Circuits and Systems, IEEE Press, 1999.
[3] E. R. Villegas, Low Power and Low Voltage Circuit Design with FGMOS Transistor, IET Circuits, Devices and Systems Series 20, 2006
[4] S. Yan and E. Sanchez-Sinencio, "Low Voltage Analog Circuit Design Techniques: A Tutorial," IEICE Trans. Analog Integrated Circuits and Systems, vol. E00-A, no. 2, pp. 1-17, Feb. 2000.
[5] J. R. Angulo, S. C. Choi and G. G. Altamirano, "Low voltage circuits building blocks using multiple input floating gate transistors," IEEE Trans. Circuits Syst.-I, vol. 42, no. 11, pp. 971-974, Nov. 1995.
[6] J. R. Angulo, G. G. Altamirano and S. C. Choi, "Modeling multiple-input floating-gate transistors for analog signal processing," Proc. IEEE Int. Symp. Circuits Syst., vol. 3, pp. 2020-2023, 1997.
[7] P. Hasler, T. S. Lande, "Overview of floating-gate devices, circuits and systems," IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing, vol.48, no.1, Jan 2001.
[8] J. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated circuits," A Design Perspective, Prentice Hall, 2003.
[9] K. Martin, "Digital Integrated circuit design," Oxford university press, Inc., 2000.
[10] B. Razavi, "Fundamentals of Microelectronics", John Wiley and sons, 2008.
[11] J. P. Uyemura, "Introduction to VLSI circuits and systems," John Wiley and sons, New Delhi, 2002.

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