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Study of Short Channel Effects for Si and GaN based n-channel FinFETs

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Abstract—This paper presents the comparative study of short channel effects (SCEs) namely Drain Induced Barrier Lowering (DIBL) and Subthreshold Swing (SS) for Si and GaN based n-FinFETs considering various gate dielectric materials such as SiO_2, SiON, Al_2O_3 and La_2O_3. These simulation results are based on the self consistent solution of Poisson and drift-diffusion equations which assumes the saturated carrier velocity in the channel for all the materials. It has been observed that GaN based n-FinFET has the excellent capability of suppressing the SCEs for all the gate dielectric materials relative to Si based n-FinFET. However, for both Si and GaN, La_2O_3 plays an effective role in reducing the DIBL and SS.

Keywords—Double gate FinFET, short channel effects (SCEs); lanthanum oxide (La_2O_3) drain induced barrier lowering (DIBL); Subthreshold swing (SS).

I. INTRODUCTION

With the advancement in themicroelectronic engineering, thetechnology oriented towards the miniaturization of electronic components and transistors in integrated circuits.Infact, the goal is to integrate more components per unit area and thus improve circuit performance while lowering their manufacturing cost. Gordon Moore in 1965 predicted that the no. of transistors in a chip doubles every two years [1]. So, in order to keep pace with this statement, the transistors size decreases from micrometer to sub-micrometer regime. The scaling of transistors can be reduced to below 20 nm to meet the predictions and goals set by the international technology roadmap for semiconductors (ITRS) [2]. As the device dimensions are scaled beyond 16 nanometer regime, conventional single gate MOSFETs experience various short channel effects (SCEs) that deteriorate the drive current and lead to off-state leakages. So, an alternative device is needed that can overcome such effectswithout deteriorating the device performance. The multi-gate transistors like FinFETs (Fin-Shaped Field Effect Transistors) are considered to be the best candidates to extend the use of CMOS technology beyond the barrier of 14 nm. Double-gate FinFET is considered one of the most promising device structures for future CMOS technology, which provides a better electrical control over the channel and thus allows increasing the device performances [3-5]. FinFET is basically a fin type FET structure and very frequently named as a double-gate transistor. It consists of a thin body of silicon wrapped by gate electrodes or poly silicon layer and the current flows in the channel from source to drain. FinFET has many advantages such as good scalability and excellent electrostatic control with promising performance for the present day nanoscale technology [6], [7]. With scaling limits and the associated SCE's of FinFETs, it seems that additional scaling down of FinFET device structure will be much more complicated because of various practical limitations, such as gate leakage through hot carrier tunneling, DIBL, SS, and threshold voltage roll-off, which can put a limit on scaling of the FinFET structures. This paper presents the simulation work of nanoscale double gate n-channel FinFET with Si and GaN as channel materials considering various high-k dielectric materials likeSiON, Al_2O_3 and La_2O_3.The impact of these gate dielectric materials on short channel effects such as sub-threshold swing (SS) and drain induced barrier lowering (DIBL) has been investigated. After investigation, it has been observed that La_2O_3 gives best results among others gate dielectrics by suppressing short channel effects (SCEs) and also has an outstanding capability of enhancing the device performance for GaN based double gate n-FinFET.

II. DEVICE STRUCTURE

A 2-D view of device structure of FinFET used in the present simulation work is as shown in Fig. 1. The device simulation has been carried out using PADRE simulator from

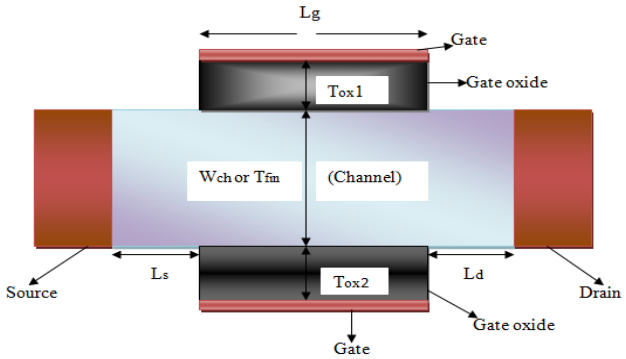

Fig.1.2-D Double-gate n-FinFET structure.

MuGFET, which is based on the drift-diffusion theory and provides self consistent solution to the poisson and drift-diffusion equations. Infact, drift and diffusion simulations are significantly faster than quantum ballistic simulations and also fairly well fitted to experimental results. The critical geometrical parameters of the FinFET are defined as below:

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1. L_g: The channel length or gate length is the final as etched length at the bottom of the gate electrode.
2. W_{ch} or T_{fin}: The channel width is defined as the separation between the two side walls or lateral gates on either side of the fin. Other nomenclatures used for channel width are fin width or fin thickness.
3. T_{ox1}, T_{ox2}: Thickness of the oxide material placed on the either side walls of fin before a gate contact is made.
4. L_s, L_d: Extension lengths to source and drain and determine the critical source/drain resistance and capacitance of device.

Table 1 shows the parameters used in simulation. Among all these dielectric materials, La_2O_3 has been observed as the best gate oxide material for GaN based double- gate FinFET as it results in reduction of SCEs such as DIBL and SS.

TABLE I.Parameters used in Simulation.

Device parameters	Values undertaken
Length of the gate (L_g)	12nm
T_{OX1} and T_{OX2}	2nm
Fin width (Wch)	10nm
Extension length to source/drain (L_s&L_d)	20nm
Channel doping	1e+16/cm^3
Drain/source Doping	1e+19/cm^3
Channel doping type	N

III. RESULTS AND DISCUSSIONS

In this section, short channel effects (SCEs) such as *Drain* Induced Barrier Lowering (DIBL) and Subthreshold Swing (SS) for double gate n-FinFethave been discussed in detail.

(A). Subthreshold Swing (SS)

One of the major parameters of the MOSFET device is subthreshold swing (SS) which determine the holding time in dynamic circuits and static power dissipation in static CMOS circuits. SS is a parameter for the calculation of leakage current and it can be expressed by the following equation:

For a MuGFET, typical value for SS parameter is 60 mV/decade i.e. 60 mV change in gate voltage brings about a tenfold change in drain current.Fig. 2 shows the subthreshold swing variation for different gate dielectric materials at V_D = 1.0 V.

$$\text{SS (mV/dec)} = \frac{dV_{GS}}{d(\log_{10} I_{DS})} \quad (1)$$

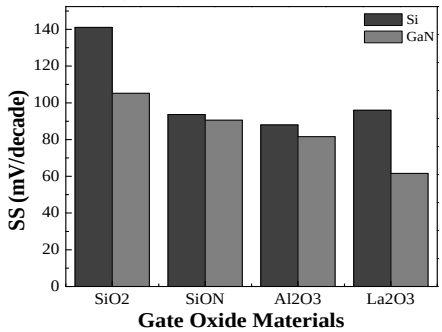

Fig. 2.Subthreshold swing variation for Si and GaN based n-FinFETs using various gate dielectrics.

For Si based n-FinFET, SS values for SiO_2, SiON, Al_2O_3 and La_2O_3 are found to be 141 mV/dec, 94 mV/dec, 88 mV/dec and 96 mV/dec respectively. However, for GaN based n-FinFET, SS values for SiO_2, SiON, Al_2O_3 and La_2O_3 are found to be 105 mV/dec, 91 mV/dec, 82 mV/dec and 62 mV/dec respectively. La_2O_3 has shown 35 % reduction in subthreshold swing for GaN based n-FinFET relative to Si based n- FinFET having gate length of 12 nm. Since SS is the parameter of calculation of leakage current, so lower the value of leakage current, lower is subthreshold swing.

(*B) Drain Induced Barrier Lowering (DIBL)*

Another short channel effect is DIBL and is defined as the reduction in the potential barrier (V_{th}) when the drain voltage (V_{DS}) is increased. The value of the DIBL can be calculated by using following expression:

$$\text{DIBL (mV/V)} = \frac{\Delta V_{TH}}{\Delta V_{DS}} \quad (2)$$

Fig. 3 shows the DIBL variation for various gate dielectric materials at V_D = 1.0 V. For Si based n-FinFET, DIBL values for SiO_2, SiON, Al_2O_3 and La_2O_3 are found to be 283 mV/V, 143 mV/V, 126 mV/V and 53 mV/V respectively. However, the DIBL values for SiO_2, SiON, Al_2O_3 and La_2O_3 are found to be 256 mV/V, 139 mV/V, 121 mV/Vand 42 mV/V respectively.

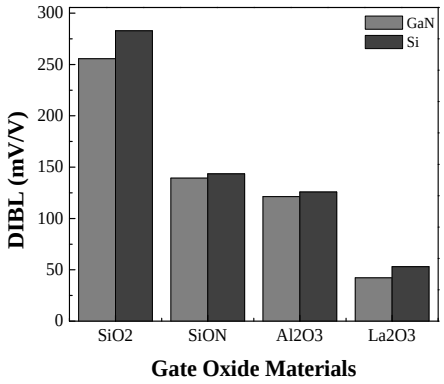

Fig. 3.DIBL variation for Si and GaN based n-FinFETs using various gate dielectrics.

La_2O_3 has shown 21 % reduction in DIBL for GaN based n-FinFET relative to Si based n-FinFET. Infact, the DIBL value for La_2O_3 is quite appreciable and reveals that it exhibits better gate control over the channel relative to other dielectric materials. Undoubtedly, gate oxide materials having high dielectric constant values are preferred for nanoscale devices.

IV. CONCLUSIONS

2-D numerical simulations using MUGFET simulator has been performed to study the performance of the FinFET based on SiO_2, HfO_2 and La_2O_3 as gate dielectric materials considering Si and GaN as channel materials. GaN based double gate n-FinFET offers effective reduction of DIBL and SS for all gate dielectric materials in comparison to Si based double gate n-FinFET. However, La_2O_3 demonstrates better performance by reducing SCEs such as sub-threshold swing

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and DIBL for double-gate n-FinFET and is amongst the best when compared to the other gate dielectric materials.

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